FILE 'HCAPLUS, WPIX' ENTERED AT 08:23:22 ON 07 JAN 2004

L1 2 S US2002055224/PN
L2 SEL L1 1- RN IC : 7 TERMS
L3 716462 S L2
L4 2 S L1 AND L3

FILE 'HCAPLUS, WPIX, JAPIO' ENTERED AT 08:29:41 ON 07 JAN 2004

L5 1956 S EDRAM OR "E"(W) DRAM OR (EMBED##### OR IMBED#####)(2A)(RAM OR DRAM OR DYNAMIC OR MEMORY) OR MEMORY DEVICES(L) EMBED#######
L6 1 S STRINGER AND L5
L7 2 S US 5622883/PN
L8 109283 S 7440-21-3(L)(POLY OR POLYCRYST?) OR POLYSI OR POLYSILICON OR POLY(W)(SI OR SILICON) OR POLYCRYST?(2A)(SI OR SILICON)
L9 241 S L5 AND L8
L10 44078 S (POLYSI OR POLYSILICON OR POLYCRYST? OR SI OR SILICON)(3A)(FRAGMENT####### OR UNWANTED OR UNDESIR###### OR PREVENT##### OR ELIMINA####### OR REMOV######## OR TRAP######## OR RETAIN##### OR HOLD##### OR HELD)
L11 26 S L9 AND L10
L12 26 S L11 NOT (L6 OR L7)
L13 SEL L12 1- IC RN : 35 TERMS
L14 1260635 S L13
L15 26 S L12 AND L14
L16 9 S L5 AND FRAGMENT######
L17 9 S L16 NOT (L15 OR (L6 OR L7))
L18 SEL L17 1- IC RN : 18 TERMS
L19 390702 S L18
L20 8 S L17 AND L19
L21 1 S L17 NOT L20
L22 109 S L5 AND SHORT#######
L23 5 S L22 AND (ISOLAT######## OR STI)
L24 94 S DUAL WORK OR DUAL WORKFUNCTION
L25 14 S L5 AND L24
L26 11 S (WORK FUNCTION OR DUAL WORKFUNCTIONS) AND L5
L27 22 S L5 AND TRAP#######
L28 3913 S GUARD RING OR GUARDRING
L29 96537 S GATE(W)(CONDUCT####### OR ELECTRODE OR METAL###)
L30 2800 S GATE(6A)(GUARD###### OR RING#####)
L31 20127 S SUPPORT#######(8A)(ARRAY###### OR MATRIX OR GRID)
L32 7927 S SUPPORT#######(8A)(STI OR ISOLAT######)
L33 12072 S (STI OR ISOLAT######)(8A)(ARRAY###### OR MATRIX OR GRID)
L34 133 S L31 AND L32
L35 86 S L33 AND L34
L36 208 S L31 AND L33
L37 131 S L32 AND L33
L38 26977 S (PROTECT###### OR PREVENT###### OR ELIMINAT##### OR TRAP#####) AND (L28 OR L29 OR L30)
L39 35 S L5 AND L38
L40 113 S L5 AND INTERCONNECT########
L41 18 S L40 AND LOCAL####
L42 125 S L5 AND (WORD OR WORDLINE)
L43 274 S L5 AND (BIT OR BITLINE)
L44 689 S L5 AND (REGION OR ZONE OR LOCATION OR POSITION OR AREA)
L45 43 S L5 AND (OVERLAY? OR OVERLI##### OR OVERLY#####)
L46 37 S (TRAP##### OR ISOLAT##### OR STI)(8A) STRINGER
L47 8746 S (TRAP##### OR ISOLAT##### OR STI)(8A)(POLYSI OR POLYSILICON OR POLYCRYST###### OR POLY)
L48 14 S (WORK FUNCTION OR WORKFUNCTION) AND L5
L49 5 S L5 AND L28
L50 105 S L5 AND L29
L51 5 S L5 AND L30
L52 53 S L5 AND (L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38)
L53 0 S L5 AND L46
L54 15 S L5 AND L47
L55 10 S L46 AND (MOSFET OR DRAM OR RAM OR MEMORY OR DYNAMIC)
L56 SEL L49 1- IC MC : 18 TERMS
L57 139986 S L56
L58 608 S L5 AND L57
L59 99 S L58 AND (ISOLAT####### OR STI)
L60 161 S L58 AND (ARRAY##### OR MATRIX##### OR GRID#####)
L61 21 S L58 AND SUPPORT########
L62 12 S L58 AND (GUARD####### OR RING##### OR TRAP######)

FILE 'HCAPLUS, WPIX, JAPIO' ENTERED AT 08:29:41 ON 07 JAN 2004

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L63      221 S STRINGER AND (MOSFET OR DRAM OR RAM OR MEMORY OR DYNAMIC)
L64        1 S L58 AND STRINGER
L65       42 S L23 OR L16 OR L15 OR (L6 OR L7)
L66      116 S (L25 OR L26 OR L27) OR L39 OR L41 OR (L48 OR L49) OR L51 OR (L54 OR L55) OR (L61 OR L62) OR L64
L67      105 S L66 NOT L65
L68       94 S L67 AND (EMBED######## OR IMBED###### OR EDRAM)
L69       34 S L68 AND (L8 OR L9 OR L10)
L70      109 S L5 AND (L28 OR L29 OR L30)
L71       24 S L5 AND (L31 OR L32 OR L33)
L72       11 S (L69 OR L71) NOT L66
L73       90 S (L25 OR L26 OR L27) OR L41 OR (L48 OR L49) OR L51 OR (L54 OR L55) OR L61 OR L64
L74        0 S L73 NOT L66
L75       82 S L73 NOT L65
L76       47 S (L69 OR L71) NOT L65
L77      103 S (L75 OR L76)
L78       12 S L77 AND L24
L79       28 S L77 AND (L28 OR L29 OR L30)
L80       23 S L77 AND (L31 OR L32 OR L33)
L81       19 S L77 AND L38
L82       16 S L77 AND L41
L83       63 S (L78 OR L79 OR L80 OR L81 OR L82)
L84        4 S L58 AND (GUARD####### OR RING##### OR PREVENT###### OR STRING##### OR FRAGMENT##### OR TRAP######)(3A)(SI
OR SILICON OR POLYSI OR POLYSILICON OR POLYCRYST?)
L85        9 S L5 AND (GUARD####### OR RING##### OR PREVENT###### OR STRING##### OR FRAGMENT##### OR TRAP######)(3A)(SI
OR SILICON OR POLYSI OR POLYSILICON OR POLYCRYST?)
L86        9 S (L84 OR L85)
L87     1652 S STRINGER/TI
L88        0 S L5 AND L87
L89       29 S (MEMORY OR DRAM OR EDRAM OR RAM OR DYNAMIC OR MOSFET OR MOS OR FET OR CMOS OR CMOSFET)/TI AND L87
L90      108 S L65 OR L83 OR L86
L91       28 S L89 NOT L90
L92    28531 S GUARDRING###### OR RING#####(4A)(PROTECT###### OR PREVENT##### OR ELIMINAT###### OR SHIELD#####)
L93     6211 S GUARDRING###### OR RING#####(4A)((POLY OR POLYCRYST?) OR POLYSI OR POLYSILICON OR SI OR SILICON)
L94     6174 S (GUARDRING###### OR RING#####)(4A)((POLY OR POLYCRYST?) OR POLYSI OR POLYSILICON OR SI OR SILICON)
L95       56 S L94 AND (EDRAM OR EMBED####### OR IMBED####### OR (DRAM OR MEMORY OR ARRAY#### OR
CELL)(3A)(SEMICONDUCT###### OR SUBSTRATE))
L96      136 S (L90 OR L91)
L97       56 S L95 NOT L96
L98        4 S L97 AND (ISOLAT####### OR STI)
L99       12 S L97 AND SUPPORT#########
L100      11 S L99 NOT L98
L101      27 S (ARRAY###### OR MATRIX)/TI AND (ISOLAT##### OR STI)/TI AND SUPPORT########/TI
L102      27 S L101 NOT (L99 OR L98 OR L96)
L103  139986 S L56
L104       2 S L102 AND (L103 OR MEMORY OR DRAM OR EDRAM OR RAM)
L105     143 S DUAL(2W) WORK OR DUAL(2W) WORKFUNCTION
L106  139986 S L56
L107      56 S L105 AND (L106 OR MEMORY OR DRAM OR EDRAM OR RAM)
L108      42 S L107 NOT (L104 OR L99 OR L98 OR L96)
L109       0 S L5 AND L108
L110      11 S L108 AND (EDRAM OR EMBED####### OR IMBED###### OR DRAM)
L111      14 S L5 AND (WORK FUNCTION OR WORKFUNCTION)
L112      14 S L111 NOT L110
L113     214 S DIVAKARUNI?/AU,IN
L114     485 S MANDELMAN, J?/IN,AU OR MANDELMAN J?/AU,IN
L115     106 S L113 AND L114
L116     106 S L113 AND L115
L117     106 S L114 AND L115
L118     106 S (L115 OR L116 OR L117)
L119  139986 S L56
L120      81 S L118 AND L119
L121      14 S L118 AND (EDRAM OR EMBED#######)
L122      83 S (L120 OR L121)
L123      11 S L122 AND (WORK OR WORKFUNCTION)
L124     219 S RADENS?/AU,IN NOT L118
L125      10 S L124 AND (WORK OR WORKFUNCTION)
L126  139986 S L56
L127     165 S L124 AND (L126 OR EDRAM OR EMBED##### OR DRAM)
L128       7 S L125 AND L126
L129       8 S L125 AND L127
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07jan04 15:39:42 User259284 Session D2561.2

DIALOG File 2:INSPEC 1969-2003/Dec W2 (c) 2003 IEE

Set	Items	Description
S1	10	EDRAM/TI
S2	4123	R1:R2
S3	328	S2 AND (EMBED???????)
S4	1232	EMBED??????(3N)(DRAM??? OR DYNAMIC OR ARRAY?????)
S5	636	S4 AND (DRAM??? OR DYNAMIC??)
S6	738	S3 OR S5 OR EDRAM??? OR EMBED?????(3N)(DYNAMIC OR DRAM???)
S7	728	S6 NOT S1
S8	14	S7 AND (GUARD???? OR SHIELD???? OR GUARDRING? OR RING??)
S9	10292	'WORK FUNCTION' OR (DUAL OR DOUBLE OR TWIN OR PAIR???)(2N) (GATE?? OR WORK OR WORKFUNCTION???)
S10	18	7AND9
S11	6	(S8 OR S10) AND (STI OR ISOLAT?????? OR INSULAT?????)
S12	56	S7 AND (ROW?? OR COLUMN???? OR GRID???? OR ARRAY?????? OR MATRIX????? OR MATRICES OR PATTERN??)(4N)(CELL?? OR MEMORY OR MEMORIES OR DRAM?? OR RAM)
S13	50	S12 AND (SUPPORT?????? OR CIRCUIT?????)
S14	7	S13 AND (STI OR ISOLAT?????? OR INSULAT?????)
S15	37	S8 OR S10:S11 OR S14
S16	16	S15 AND DUAL
S17	11	S15/2001-2004
S18	26	S15 NOT S17
S19	32	S16 OR S18
S20	32	S19 NOT S1
S21	0	EDRAM?? AND STRINGER?
S22	2	DRAM?? AND STRINGER?
S23	11101	(EDRAM??? OR DRAM??? OR DYNAMIC) AND SHORT?????
S24	291	S23 AND ARRAY????????
S25	9	S24 AND (EDRAM?? OR (EMBED???? OR IMBED???? OR BURY????? OR BURIED)(4N)(ARRAY???? OR CELL?? OR DRAM OR MEMORY OR SUBSTRATE??))
S26	1	(POLYSI OR POLYCRYST? OR POLY OR SI OR SILICON)(2N)STRINGER???
S27	35	S6 AND (FAIL?????? OR DEFECT??????)/TI,DE,ID
S28	7	S27 AND ARRAY?????????

AN 2003-016080 [01] WPIX
CR 2003-327882 [31]
DNN N2003-012004 DNC C2003-003896
TI Capacitor manufacturing method for DRAM, SRAM, involves removing portion of insulating layer formed between through-holes to separate conductor in insulated sidewall from one electrode to other electrode.
IN BURKE, R J; TANG, S D
PA (BURK-I) BURKE R J; (TANG-I) TANG S D; (MICR-N) MICRON TECHNOLOGY INC
PI US 2002109170 A1 20020815 (200301)* 16p H01L027-108 <--
US 6599799 B2 20030729 (200354) H01L021-8242 <--
PRAI US 2000-569570 20000510; US 2002-117036 20020408

AB US2002109170 A UPAB: 20030821
NOVELTY - A conductor is formed in an insulated sidewall of a through-hole provided on an insulating layer (32). A capacitor with a dielectric layer (92) is formed between a pair of conductive electrode in another through-hole. A portion of the insulating layer between the through-holes, is removed, such that the insulated sidewall and one of the electrodes separate the conductor from the other electrodes.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) DRAM cell array manufacturing method;
(2) Semiconductor device manufacturing method;
(3) Semiconductor device;
(4) DRAM cell array;
(5) Processor-based system; and
(6) **Embedded memory** processor-based system.

USE - For forming double-sided container capacitor for dynamic random access memory (DRAM), static random access memory (SRAM) used in processor-based system (claimed) e.g. computer system.

ADVANTAGE - The closely-spaced double-sided stacked capacitor improves the alignment tolerance for bit line contact formation and increases the overall feature density of the circuit die with enhanced device performance.

DESCRIPTION OF DRAWING(S) - The figure shows a **fragmentary** vertical cross-sectional view of the DRAM cell array.

Insulating layer 32
Dielectric layer 92

Dwg.9/12

L83 ANSWER 51 OF 63 WPIX
AN 2001-595751 [67] WPIX
DNN N2001-444029 DNC C2001-176354
TI Silicon oxide layer etching without damaging underlying silicon nitride layer in integrated circuit device fabrication, involves **protecting** silicon nitride spacers by photoresist layer when etching.
IN LEE, Y
PA (LEEY-I) LEE Y; (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
PI US 2001018165 A1 20010830 (200167)* 11p G03F007-00
US 6586162 B2 20030701 (200345) G03F007-00
PRAI US 2000-729624 20001201; US 1998-35050 19980305
IC ICM G03F007-00
AB US2001018165 A UPAB: 20011119

NOVELTY - **Polysilicon gate electrodes** (PGE) (16) are formed on substrate (10), and silicon nitride spacers are formed on sidewalls of PGE. Silicon oxide layer (SOL) is deposited on PGE, and SOL is covered with photoresist layer (PL). PL is developed until SOL is exposed. The exposed SOL is etched to expose PGE, and to **protect** spacers by remaining PL. The remaining PL is then removed, and IC device is fabricated.

DETAILED DESCRIPTION - Silicon oxide layer with a thickness of 200-500 Angstrom is covered with photoresist layer having thickness of 1300-2700 Angstrom . The photoresist layer is developed using trimethyl ammonium hydroxide until the silicon oxide layer is exposed, and remaining photoresist layer is below the top of **polysilicon gate electrodes**. The exposed silicon oxide layer is etched without using a masking process, by wet-etching method having high selectivity for silicon oxide with respect to silicon nitride so that the silicon nitride spacers are not damaged during etching.

An INDEPENDENT CLAIM is also included for fabrication of integrated circuit device.

USE - For etching silicon oxide layer without damaging underlying silicon nitride layer in fabrication of integrated circuit device (claimed).

ADVANTAGE - The method provides an inexpensive, easily controllable process to expose areas of wafer for silicidation while **protecting** other areas. The silicon oxide layer is etched without damaging the underlying silicon nitride spacers. The method is used for **embedded dynamic** random access memory (**EDRAM**) manufacture in which both memory and logic circuits are fabricated on the same wafer. Since the silicon nitride sidewall spacers are not damaged by etching process, bridging does not occur. Provides effective salicide (self-aligned silicide) formation process in fabrication of integrated circuits. The method enables to form salicided gate and source/drain regions in the logic circuits of **embedded memory** integrated circuit device using resist planarization, while **protecting** areas within the memory circuits that are not to be silicided.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view

of fabricated **EDRAM** device.
Semiconductor substrate 10
Polysilicon gate electrodes 16
Dwg.11/11
KW [1] 413-0-0-0 CL USE; 219-0-0-0 CL; 0047-18201 CL USE

L20 ANSWER 3 OF 8 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2003-327882 [31] WPIX
CR 2003-016080 [01]
DNN N2003-262160 DNC C2003-085224
TI Dynamic random access memory cell array comprises dynamic random access memory cell capacitor(s) having dielectric layer between first and second conductive electrodes.
IN BURKE, R J; TANG, S D
PA (MICR-N) MICRON TECHNOLOGY INC
PI US 6507064 B1 20030114 (200331)* 14p H01L027-108 <--
PRAI US 2000-569570 20000510
AB US 6507064 B UPAB: 20030516
NOVELTY - A dynamic random access memory (DRAM) cell array comprises a DRAM cell capacitor having a dielectric layer between first and second conductive electrodes. The capacitor is formed adjacent an insulated sidewall (54) such that only the insulated sidewall and a dielectric layer (92) separate the conductor from the second electrode.

DETAILED DESCRIPTION - A DRAM cell array comprises: a conductor(s) with an insulated sidewall formed over a semiconductor structure; and a DRAM cell capacitor having a dielectric layer between first and second conductive electrodes. The capacitor is formed adjacent the insulated sidewall such that only the insulated sidewall and the dielectric layer separate the conductor from the second electrode.

INDEPENDENT CLAIMS are also included for the following:

(a) a semiconductor device provided with a capacitor comprising: a semiconductor structure; a conductor formed over the semiconductor structure; and a capacitor having a dielectric layer formed between first and second electrodes;

(b) a processor-based system comprising: a processor; a memory circuit connected to the processor, where the memory circuit includes a semiconductor device; and

(c) an **embedded-memory** processor-based system comprising: a processor; and a memory circuit formed over a same integrated circuit as the processor, where the memory circuit includes a semiconductor device comprising a conductor and a capacitor.

USE - None given.

ADVANTAGE - The DRAM cell array exhibits improved alignment tolerance, and has a reduced overall stacked height.

DESCRIPTION OF DRAWING(S) - The figure is a **fragmentary** vertical cross-sectional view of the array.

First insulating layer 32
Cell plug 34
Bit line plug 38
Insulated sidewall 54
Bit line contact plug 62
Dielectric layer 92
Dwg.9/12
TECH US 6507064 B1 UPTX: 20030516
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The DRAM cell capacitor is a double-sided DRAM cell capacitor. The insulated sidewall is

formed of an insulating material which selectively stops a wet etch. The conductor is formed of a conductive material which selectively stops the wet etch. The second electrode is formed of a conductive material which stops the wet etch. The first electrode is in electrical contact with a conductive cell plug (34) in the structure.
The semiconductor device further comprises: a first insulating layer (32) overlying at least a portion of a semiconductor structure; and a bit line contact plug (62) having an insulated sidewall formed adjacent to the capacitor. The bit line contact plug is in electrical contact with a conductive bit line plug (38) in the structure.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The second conductive electrode is made of doped polysilicon. The insulated sidewall is made of silicon nitride. The conductor is made of tungsten or doped polysilicon. The cell plug and the bit line plug are made of doped or doped hemi-spherical grain polysilicon. The bit line contact plug is made of tungsten or doped polysilicon.

FS CPI EPI

FA AB; GI

L123 ANSWER 11 OF 11 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-125967 [14] WPIX
DNN N2001-092850 DNC C2001-036756
TI Manufacture of a metal oxide semiconductor field effect transistor by exposing the implanted base wafer, forming a gate dielectric layer on the exposed base wafer, covering the implanted gate structure with a refractory metal deposit.
IN **DIVAKARUNI, R**; GAMBINO, J P; **MANDELMAN, J**; RENGARAJAN, R; **MANDELMAN, J A**
PA (IBMC) IBM CORP; (INFN) INFINEON TECHNOLOGIES AG; (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP

PI	EP 1071125	A2	20010124	(200114)*	EN	21p	H01L021-336
	JP 2001068672	A	20010316	(200121)		17p	H01L029-78
	CN 1286495	A	20010307	(200140)			H01L021-336
	KR 2001039731	A	20010515	(200167)			H01L029-772
	US 6501131	B1	20021231	(200305)			H01L029-76
	TW 516232	A	20030101	(200355)			H01L029-772

PRAI US 1999-359291 19990722
AB EP 1071125 A UPAB: 20030828
NOVELTY - A metal oxide semiconductor field effect transistor (MOSFET) is made by etching nitride and polysilicon layers in a layered structure; forming spacers; implanting and exposing base wafer; forming a gate dielectric layer on the exposed base wafer; covering the implanted gate structure with a refractory metal deposit.

DETAILED DESCRIPTION - Manufacture of a MOSFET comprises:

(a) forming a layered structure comprising a nitride layer covering a polysilicon layer that covers a sacrificial oxide layer (1);

(b) etching the nitride layer and the polysilicon layer to form an opening with sidewalls extending into the sacrificial oxide layer;

(c) forming spacers on the sidewalls (13) on the opening;

(d) implanting the base wafer (2) to set a threshold voltage for the MOSFET;

(e) stripping the spacers and the sacrificial oxide layer from the opening to expose the base wafer;

(f) forming a gate dielectric layer (12) on the exposed base wafer, filling bottom portions of the opening with a doped gate structure (14);

(g) implanting the doped gate structure to set a **work** -function for the gate structure; and

(h) covering the implanted gate structure with a refractory metal deposit. The layer structure is between opposing raised shallow trench isolation regions.

An INDEPENDENT CLAIM is also included for a MOSFET structure comprising:

(a) a layered gate structure with an oxide cap covering the refractory metal deposit that covers the doped gate structure over the gate dielectric layer that covers the base wafer;

(b) source/drain extension implants;

(c) an implanted punch-through stop pocket; and

(d) an implant setting a threshold voltage.

USE - For manufacturing a MOSFET structure.

ADVANTAGE - The invention provides (a) dual **work**-function doping following the customary gate sidewall oxidation step of the manufacturing process, greatly reducing thermal budget and boron penetration concerns; (b) reduced aspect ratios while maintaining a low sheet resistance; and (c) an improved MOSFET having improved channel structure, electrical characteristics, reduced short channel effect, lower junction capacitance, reduced junction leakage, and improved hot-carrier reliability.

DESCRIPTION OF DRAWING(S) - The figure shows the MOSFET structure.

Sacrificial oxide layer 1
Base wafer 2
Gate dielectric layer 12
Sidewalls 13
Gate structure 14
Nitride layer 20
Dwg.9/21

TECH EP 1071125 A2 UPTX: 20010312

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The nitride layer is etched with a directional anisotropic etching selective to silicon. The directional anisotropic etching is a reactive ion etching. The polysilicon layer is etched with a reactive ion etching selective to nitride and oxide. Preferred Component: The spacers are formed of a material containing a P-type dopant. The source/drain extension implants are set with a doping type independent from that of the gate structure. The doped gate structure incorporates dual **work**-function gate doping.
Preferred Device: The MOSFET structure defines a gated array MOSFET. The MOSFET further comprises (a) doping pockets for determining the threshold voltage; and (b) borderless contact formed over the MOSFET structure. The doping pockets are positioned to produce a doping concentration adjacent to the sidewalls higher than a doping concentration produced toward the center portion of the layered gate structure. The borderless contact includes (i) a thin nitride layer (20) deposited over the MOSFET structure so that the nitride layer conforms to underlying features of the structure; (ii) an opening formed in the thin nitride layer in an area for receiving the borderless contact; and (iii) a polysilicon layer deposited over the opened area and patterned to form a landing pad region for receiving a contact.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The base wafer is silicon. The nitride layer is silicon nitride. The gate dielectric is formed of dielectric materials comprising a thermally grown silicon dioxide, a nitride gate oxide, and a deposited dielectric film. The refractory metal comprises tungsten, tantalum, molybdenum, and the silicides of tungsten, tantalum, and molybdenum.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Material: The spacer material is borosilicate glass.

FS CPI EPI
FA AB; GI
MC CPI: L04-C02B; L04-C07A; L04-C10F; L04-C12A; L04-C

L123 ANSWER 7 OF 11 WPIX
AN 2002-328903 [36] WPIX
CR 2002-236981 [29]
DNN N2002-258148 DNC C2002-094991
TI Fabrication of semiconductor structure by providing substrate, conductor comprising intrinsic polysilicon, and insulating cap, doping portions of intrinsic polysilicon, and forming gate sidewall layer having bird's beak.
IN **DIVAKARUNI, R; MANDELMAN, J A**
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 2002028559 A1 20020307 (200236)* 17p H01L021-336
US 6432787 B1 20020813 (200261) H01L021-336
PRAI US 1999-325943 19990604; US 2001-982822 20011022
AB US2002028559 A UPAB: 20020924

NOVELTY - Semiconductor structure is fabricated by providing a semiconductor substrate, a gate insulator, a conductor comprising intrinsic polysilicon, a silicide layer and an insulating cap; forming insulating spacers along the sides of silicide layer and insulating cap; doping portions of intrinsic polysilicon; and forming a gate sidewall layer including a bird's beak.

DETAILED DESCRIPTION - Fabrication of a semiconductor structure includes providing a semiconductor substrate (5), a gate insulator (10), a conductor comprising intrinsic polysilicon (11), a silicide layer (12) and an insulating cap (13). Insulating spacers are provided along the sides of silicide layer and insulating cap. Portions of intrinsic polysilicon are doped with a first conductivity-type dopant. A gate sidewall layer including a bird's beak is formed on the sides of polysilicon.

USE - For fabricating semiconductor structure.

ADVANTAGE - Achieves dual **work** function requirement by applying either P+ or N+ doping to the gate conductor while creating self-aligned cap on the gate conductor. The dual **work** function gates in the support region allow surface channel metal-oxide semiconductor field-effect transistor for high performance.

DESCRIPTION OF DRAWING(S) - The drawing shows a semiconductor structure.

substrate 5
gate insulator 10
intrinsic polysilicon 11
silicide layer 12
insulating cap 13

Dwg.4A/12

TECH US 2002028559 A1UPTX: 20020610

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The first conductivity-type dopant is spread over the intrinsic polysilicon to form a first-doped polysilicon layer. The method may include etching portions of the first doped polysilicon layer, covering the other portions of the semiconductor structure with a block mask while etching, doping the other portions of the intrinsic polysilicon with a second conductivity-type dopant, spreading the second conductivity-type dopant over the polysilicon to form a second doped polysilicon layer, and adding first and/or second conductivity-type dopant to the substrate to form source-drain extensions.

Doping of the other portions of the intrinsic polysilicon creates source-drain contact regions in the substrate.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The insulating layer comprises silicon nitride.

FS CPI EPI
FA AB; GI
MC CPI: L04-C02B; L04-C10B; L04-C12C

L83 ANSWER 43 OF 63 WPIX
AN 2002-443196 [47] WPIX
DNN N2002-349135 DNC C2002-126114
TI Deposition of conformal hydrogen-rich silicon nitride onto patterned structure involves rapid thermal chemical vapor deposition or low pressure chemical vapor deposition using silicon precursor-based chemistry.
DC L03 U11 U13
IN BALSAN, C; BUCHET, C; RAFFIN, P; THIOLIERE, S
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP

PI	US 2002039835 A1	20020404	(200247)*	21p	H01L021-44
	JP 2002110673 A	20020412	(200247)	17p	H01L021-318
	KR 2002009418 A	20020201	(200254)		H01L021-318
	TW 473829 A	20020121	(200308)		H01L021-205

PRAI EP 2000-480071 20000725
AB US2002039835 A UPAB: 20020725

NOVELTY - Depositing a conformal hydrogen-rich silicon nitride layer onto a patterned structure comprises rapid thermal chemical vapor deposition (RTCVD) using a silicon precursor-based chemistry at 600-950 deg. C and 50-200 Torr or low pressure chemical vapor deposition (LPCVD) using silicon precursor-based chemistry at 640-700 deg. C and 0.2-0.8 Torr.

DETAILED DESCRIPTION - Depositing a conformal hydrogen-rich (H-rich) silicon nitride (Si3N4) layer (21) onto a patterned structure comprises providing a patterned structure comprising a silicon substrate (11) coated with a thin silicon dioxide (SiO2) gate layer having **gate conductor** (GC) lines (16) and having diffusion region(s) formed between two adjacent GC lines. A conformal H-rich Si3N4 layer is deposited onto the structure in a rapid thermal chemical vapor deposition (RTCVD) reactor using a silicon (Si) precursor-based chemistry at 600-950 deg. C and 50-200 Torr. An INDEPENDENT CLAIM is also included for a method of fabricating a borderless **polysilicon** contact with a diffusion region in a silicon substrate by depositing a conformal H-rich Si3N4 layer onto a patterned structure; depositing a layer of borophosphosilicate (BPSG) material in excess onto the structure to fill spaces between the GC lines; planarizing the BPSG material by chemical-mechanical polishing to remove the BPSG down to the Si3N4 cap surface; depositing a passivating layer of tetraethylorthosilicate (TEOS) SiO2 onto the structure; defining a photolithography mask to expose contact hole locations; anisotropically dry etching the TEOS SiO2, BPSG, Si3N4 and SiO4 materials in sequence to expose the diffusion region to form the contact hole; and depositing doped **polysilicon** to fill the contact hole and create the borderless **polysilicon** contact with the diffusion region.

USE - For depositing a conformal H-rich Si3N4 layer onto a patterned structure in the fabrication of a borderless **polysilicon** contact with a diffusion region in a silicon substrate.

ADVANTAGE - The conformal and hydrogen-rich layer **prevents** junction leakage in **embedded dynamic** random access memory (**EDRAM**) and synchronous dynamic random access memory (SDRAM) silicon chips. It has a uniform thickness across the wafer irrespective the **array** or **support** area. The invention provides lower contact resistance, larger process window, throughput

improvements and process flow simplification.
DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of a structure undergoing the essential steps of borderless **polysilicon** contact fabrication when the silicon nitride barrier layer is deposited according to the method of the invention.
Substrate 11
GC lines 16
Si3N4 layer 21
Dwg.4/7

TECH US 2002039835 A1UPTX: 20020725
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The Si precursor-based chemistry is silane (SiH4) or silane/ammonia (SiH4/NH3) mixture. For LPCVD, the silicon precursor-based chemistry is dichlorosilane (DCS), NH3/DCS mixture or NH3/SiH4/DCS mixture.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The deposition is performed in an AME Centura tool with a carbon susceptor **protected** against nitrogen trifluoride (NF3) at 90 Torr and 785degreesC with SiH4 flow of 0.2 L/min, NH3 flow of 3 L/min and nitrogen flow of 10 L/min and at a deposition rate of 90 nm/min.

FS CPI EPI

L129 ANSWER 4 OF 8 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-452820 [48] WPIX
DNN N2002-356973 DNC C2002-128739
TI Fabrication of semiconductor devices, e.g., transistors, involves forming gate conductor material layers on oxide layers formed on doped channel region.
IN HSU, L L; MANDELMAN, J A; **RADENS, C J**; TONTI, W R; WANG, L
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 6355531 B1 20020312 (200248)* 16p H01L021-8236
TW 511228 A 20021121 (200353) H01L021-76
PRAI US 2000-634225 20000809
AB US 6355531 B UPAB: 20020730

NOVELTY - A semiconductor device is fabricated on a substrate by forming gate conductor material layer on an oxide layer formed on a doped channel region.

DETAILED DESCRIPTION - Fabrication of semiconductor device on a substrate, involves (a) defining channel regions in the substrate; (b) forming various types of doped channel regions by performing in sequence various channel implant processes with respect to the channel regions; (c) forming an oxide layer (OL) on each of the doped channel regions; and (d) forming a gate conductor material layer on the oxide layer. The gate conductor material layer determines a gate conductor **work** -function of the corresponding semiconductor devices (D1, D2, D3). Each of the various types of doped channel region has a different doping level determined by the corresponding channel implant processes which are free from an implant mask.

USE - For fabricating semiconductor device, e.g., metal oxide field effect transistors (MOSFETs).

ADVANTAGE - The device provides flexibility in designing electronic circuitry, thus designers have much wider range of device types from which to choose. Also, since the method does not require multiple masks or masking processes, it costs less as compared with conventional methods.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of semiconductor devices where gate side-walls are formed on the side surface of the gate conductors.

Semiconductor devices D1, D2, D3
Gate conductor material GC1, GC2, GC3
Gate conductors GT1, GT2, GT3
Oxide layer OL
Side-wall oxide layer SO
Sidewall spacer SS
Dwg.9/9

TECH US 6355531 B1 UPTX: 20020730

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The various types of doped channel regions are formed by performing a first maskless implant process with respect to channel regions, performing a second maskless implant process with respect to the channel regions including the channel region covered with a gate conductor material (GC1, GC2, GC3) layer, and performing a third maskless implant process with respect to the channel regions including the first type doped channel region and the channel

region covered with another gate conductor material layer. The method further includes recessing the gate conductor material layer and forming layer(s) on each of the recessed gate conductor material layers to form a gate conductor. The step of forming the layer(s) on the gate conductor material layer includes forming a silicide layer on each of the recessed gate conductor material layer and forming an oxide layer on the silicide layer. The step of forming the layer(s) may also include depositing refractory metal on surface of each of the recessed N gate conductor material layers, reacting the refractory metal with poly gate, and removing unreacted metal using a selective etching process. An interlayer conductive diffusion barrier is further formed between the layer(s) and each of the recessed gate conductor material layers. The silicon nitride layers surrounding the gate conductors (GT1, GT2, GT3) are removed, followed by forming gate sidewalls on side surfaces of each gate conductor, forming a side-wall oxide layer (SO) on each side surfaces, and forming a sidewall spacer (SS) on the sidewall oxide layer. A source-drain junction implantation is performed in each semiconductor device independent of a gate **work**-function of the semiconductor device.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The interlayer conductive diffusion barrier can be titanium nitride or tantalum silicon nitride.

FS CPI EPI

FA AB; GI

MC CPI: **L03-G04A**; L04-C02; L04-C12; **L04-E01B1**

L23 ANSWER 4 OF 5 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-266396 [31] WPIX
CR 2003-800788 [75]
DNN N2002-206962 DNC C2002-079249
TI Salicide FET fabrication method for e.g. embedded SRAM, involves ion-implanting contact dopant in borderless contact openings in period between two rapid thermal annealing steps.
IN LEI, M; THEI, K; WUU, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
PI US 6335249 B1 20020101 (200231)* 8p H01L021-336
PRAI US 2000-498981 20000207
AB US 6335249 B UPAB: 20031120

NOVELTY - A silicide layer is formed on gate electrodes (16) and source/drain contact areas (19) selectively by rapid thermal annealing (RTA).

Etch stop layer (24) and interlevel dielectric (ILD) layer (28) are deposited, and borderless contact openings are etched in the ILD layers.

A contact dopant is implanted in the contact openings and substrate (10) and then, final RTA is carried out.

USE - For fabrication of salicide N-channel and P-channel FETs for CMOS circuits and **embedded memory devices** such as **embedded** SRAM and **embedded DRAM**.

ADVANTAGE - The ion implantation of contact dopants during a period between two RTA processes, results in modified source/drain contact diffused junction profile in the silicon substrate below and adjacent to over-etched field oxide regions, at the shallow trench **isolation** substrate interface. Hence reduces source/drain-to-substrate electrical **shorts**.

Enables manufacturing N-channel and P-channel FETs having improved borderless contacts simultaneously on same substrate. Provides improved borderless contact structure without increasing the thermal limits, and requires simple and cost effective manufacturing process, provides substantially higher product yields.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross sectional view of salicide FET during manufacturing process.

Substrate 10
Gate electrode 16
Source/drain contact areas 19
Etch stop layer 24
Interlevel dielectric layer 28

Dwg.5/5

TECH US 6335249 B1 UPTX: 20020516

TECHNOLOGY FOCUS - ORGANIC CHEMISTRY - Preferred Process: The unreacted metal layer after thermal annealing, is removed by selective etching in a solution of ammonium hydroxide, hydrogen peroxide and water.

FS CPI EPI
FA AB; GI

L83 ANSWER 44 OF 63 WPIX
AN 2002-412780 [44] WPIX
DNN N2002-324281
TI Manufacturing method of **embedded** type **dynamic** random access memory - with the capability of solving the falling off problem of **guard-ring** without increasing the step of process.
IN CHANG, C; CHU, T; YEN, Y
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
PI TW 451474 A 20010821 (200244)* H01L027-108
PRAI TW 2000-114505 20000720
AB TW 451474 A UPAB: 20020711

NOVELTY - The present invention provides the manufacturing method of **embedded** type **dynamic** random access memory. First, the first conducting layer is formed on the semiconductor substrate surface of the logic circuit region. Then, the second conducting layer is formed to cover the first conducting layer and the semiconductor substrate surface of memory cell region. In addition, the second conducting layer has the first height drop. After that, a shielding layer, which has the second height drop corresponding to the first height drop, is formed on the second conducting layer surface. The first photoresist mask is formed at the position that is desired for forming the gate on the memory cell region. The second photoresist mask is formed at the same time to cover the position of the second height drop. By using the first and the second photoresist masks as the blocking materials, the shielding layer is etched until the second conducting layer is exposed so as to form the first blocking material and the second blocking material. Based on the manufacturing method of this invention, the falling off problem of **guard-ring** can be effectively solved under the condition that the step of process is not increased.
Dwg.0/0

FS EPI
FA AB

L83 ANSWER 2 OF 63 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:954406 HCAPLUS
ED Entered STN: 08 Dec 2003
TI Manufacturing method of **embedded** type **dynamic** random access memory
IN Chu, Tsu-Yu; Yen, Yi-Tung; Chang, Chai-Der
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 5 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
IC ICM H01L027-108
CC 76 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 451474	B	20010821	TW 2000-89114505	20000720
				TW 2000-89114505	20000720

AB The present invention provides the manufg. method of **embedded** type **dynamic** random access memory. First, the first conducting layer is formed on the semiconductor substrate surface of the logic circuit region. Then, the second conducting layer is formed to cover the first conducting layer and the semiconductor substrate surface of memory cell region. In addn., the second conducting layer has the first height drop. After that, a shielding layer, which has the second height drop corresponding to the first height drop, is formed on the second conducting layer surface. The first photoresist mask is formed at the position that is desired for forming the gate on the memory cell region. The second photoresist mask is formed at the same time to cover the position of the second height drop. By using the first and the second photoresist masks as the blocking materials, the shielding layer is etched until the second conducting layer is exposed so as to form the first blocking material and the second blocking material. Based on the manufg. method of this invention, the falling off problem of **guard-ring** can be effectively solved under the condition that the step of process is not increased.

L83 ANSWER 46 OF 63 WPIX
AN 2002-225220 [28] WPIX
CR 2001-298951 [31]
DNN N2002-172644 DNC C2002-068650
TI Manufacture of semiconductor device involves forming thin thermally-oxidized **polysilicon** side-wall film that blocks oxidation of refractory metal nitride barrier layer.
IN CUNNINGHAM, J A
PA (PHIG) PHILIPS SEMICONDUCTORS INC; (PHIG) KONINK PHILIPS ELECTRONICS NV
PI US 2001013600 A1 20010816 (200228)* 10p H01L021-331
US 6479362 B2 20021112 (200278) H01L021-331
PRAI US 1998-136482 19980819; US 2001-783689 20010214
AB US2001013600 A UPAB: 20021204

NOVELTY - A semiconductor device is made by forming a thin thermally-oxidized **polysilicon** side-wall film (114a, 114b) against underlying doped **polysilicon** layer, metal nitride barrier layer (108), overlying silicide layer, and cap dielectric. The sidewall film is arranged to block oxidation of the thin refractory metal nitride barrier layer.

DETAILED DESCRIPTION - Manufacture of semiconductor device having a polycide transistor **gate electrode** involves:

(a) forming a thin refractory metal nitride barrier layer between doped **polysilicon** layer and overlying silicide layer to reduce diffusion transport of dopants between them; and

(b) forming a thin thermally-oxidized **polysilicon** side-wall film against the underlying doped **polysilicon** layer, the metal nitride barrier layer, the overlying silicide layer, and the cap dielectric. The sidewall film is arranged to block oxidation of the thin refractory metal nitride barrier layer.

USE - For forming complementary metal oxide semiconductors for high-performance logic applications such as microprocessors or **embedded dynamic** random access memory implementations.

ADVANTAGE - The method provides improved **gate electrode** exhibiting greater tolerances to higher temperature annealing treatments. It avoids threshold voltage shifts and possible poly-depletion problems caused by rapid diffusion of dopants. It also **prevents** silicide agglomeration which in turn **prevents** resistivity increase. It further solves the problem of increased junction leakage of the prior art.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a semiconductor gate structure.

Refractory metal nitride barrier layer 108

Sidewall film 114a, 114b

Dwg.1/4

TECH US 2001013600 A1UPTX: 20020502

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Process: The nitride side-wall film is formed after photolithographic patterning. Ionic dopants are implanted in the source and drain regions after the patterning step. The process also involves forming spacers against the **polysilicon** side-wall film, and then reoxidizing the spacers. A conductive layer is

also formed as part of self-aligned contact structure. A bird's beak is as well formed at the lower edge of the underlying **polysilicon** film. The **polysilicon** film is oxidized to form an oxide layer.
The process further involves implanting second ionic dopants in source and drain regions, and activating the dopants at elevated temperature to uniformly distribute the ionic dopants.
Preferred Material: The thin refractory metal nitride barrier layer includes titanium, and tungsten. The cap dielectric is formed of silicon oxide, or silicon nitride. The spacers are formed of silicon oxide, or silicon nitride. The metal nitride film includes zirconium and titanium.
FS CPI EPI
FA AB; GI

20/9/7

DIALOG(R)File 2:INSPEC

6959813 INSPEC Abstract Number: B2001-08-1265D-001

Title: **Dual**-thickness **gate** oxidation technology with halogen/xenon implantation for **embedded dynamic** random access memories

Author(s): Sugizaki, T.; Murakoshi, A.; Ozawa, Y.; Nakanishi, T.; Suguro,K.
Author Affiliation: Fujitsu Labs. Ltd., Yokohama, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.40, no.4B p.2674-8
Publisher: Japan Soc. Appl. Phys,
Publication Date: April 2001 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(200104)40:4BL.2674:DTGO;1-D
Material Identity Number: F221-2001-010
Conference Title: 1999 International Conference on Solid State Devices and Materials (SSDM'99)
Conference Date: 29-31 Aug. 2000 Conference Location: Sendai, Japan
Language: English Document Type: Conference Paper (PA); Journal Paper
Treatment: Experimental (X)

Abstract: We investigated the enhanced oxidation effect of using silicon (Si) implanted with fluorine (F), iodine (I), and xenon (Xe) before gate oxidation. I and Xe, which result in shallower implants because of their higher mass numbers, were expected to be less damaging to the Si substrate. The resultant increase in oxide thickness was found to be 20%, 80%, and 50% under F, I, and Xe implantations with a dose of 5*10/sup 14/ cm/sup -2/, respectively. We found that F atoms outdiffuse to their ambient through SiO/sub 2/, and that i implantation causes the greatest increase in oxide thickness. In addition, F implantation shows highly reliable dielectric characteristics, low contact resistance, and a low junction leakage current. Consequently, the F implantation process is capable of providing reliable **dual**-thickness **gate** oxide for **embedded dynamic** random access memories (**DRAMs**). (6 Refs)

Subfile: B

20/9/5
DIALOG(R)File 2:INSPEC

7183502 INSPEC Abstract Number: B2002-03-2550B-042
Title: Effect of N+ ion implantation and Gox process on In and B channel profile
Author(s): Curello, G.; Rengarajan, R.; Faul, J.; Wurzer, H.; Amon, J.; Gaertner, T.; Henke, D.; Schmeide, M.; Kieslich, A.
Author Affiliation: Technol. Dev. Dept., Infineon Technol. AG, Dresden, Germany
Conference Title: Si Front-End Processing - Physics and Technology of Dopant-Defect Interactions II. Symposium (Materials Research Society Proceedings Vol.610) p.B3.4.1-6
Editor(s): Agarwal, A.; Pelaz, L.; Vuong, H.-H.; Packan, P.; Kase, M.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 2001 Country of Publication: USA xv+416 pp.
ISBN: 1 55899 518 8 Material Identity Number: XX-2001-01170
Conference Title: Si Front-End Processing - Physics and Technology of Dopant-Defect Interactions II. Symposium
Conference Date: 24-27 April 2000 Conference Location: San Francisco,
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: The effect of different **dual gate** oxide (DGox) processes on the electrical properties of CMOS devices in deep submicron **embedded DRAM** (**eDRAM**) technology is reported. Also discussed, is the effect of N/sup +/ ion implantation on the diffusion/segregation behaviour of B and In channel dopants. In particular, it is shown that the N/sup +/ dose required to obtain a certain combination of **dual gate** oxide thickness varies with the gate oxide process. Effects of N/sup +/ dose on the In and B channel profiles are studied using SIMS. The impact of "thickness-equivalent" DGox processes on short channel effect (SCE) and carrier mobility is analyzed and tradeoffs for optimization of device performances are discussed. (17 Refs)
Subfile: B

L123 ANSWER 8 OF 11 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-236981 [29] WPIX
CR 2002-328903 [23]
DNN N2002-182289 DNC C2002-071660
TI Semiconductor structure for field effect transistor, comprises semiconductor substrate, gate insulator, doped polysilicon layer, silicide layer, insulating cap, and gate sidewall.
IN **DIVAKARUNI, R; MANDELMAN, J A**
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 6333220 B1 20011225 (200229)* 16p H01L021-8242 <--
PRAI US 1999-325943 19990604
AB US 6333220 B UPAB: 20020610
NOVELTY - A semiconductor structure comprises a semiconductor substrate; a gate insulator over the substrate; a doped polysilicon layer on the insulator; a silicide layer on the doped polysilicon layer; an insulating cap on the silicide layer; and gate sidewall layer on sides of the doped polysilicon layer. The sidewall layer has bird's beak at the corner of the doped polysilicon layer.
USE - For field effect transistor.
ADVANTAGE - The structure forms dual **work** functions doping with self-aligned insulating gate conductor cap that minimizes gate induced drain leakage. The bird's beak reduces gate to diffusion overlap capacitance, which results in reduced bitline capacitance and improved performance. It also allows formation of borderless diffusion contacts in the array region for high density.
Dwg.0/12
TECH US 6333220 B1 UPTX: 20020508
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Device: The structure also comprises silicon nitride spacers on the sides of silicide layer and insulating cap; and source-drain contact regions in the substrate. It also includes a second insulator, second doped polysilicon layer, a second silicide layer, and a second insulating cap.
Preferred Property: The second doped polysilicon layer is doped with either first or second conductive type dopants. The source-drain regions are formed by second conductive type dopants.
FS CPI EPI
FA AB
MC CPI: L04-C02; L04-C10F; L04-C12; L04-E01A
EPI: U11-C05B9B; U11-C08A2; **U12-D02A**

L83 ANSWER 49 OF 63 WPIX
AN 2001-616013 [71] WPIX
DNN N2001-459560
TI Trench capacitor is formed by forming trench in substrate, and lining walls of the trench with semiconductor material having uniform thickness over sidewalls.
IN GRUENING, U; RADENS, C J; SCHREMS, M
PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP

PI WO 2001045162	A1	20010621	(200171)*	EN	52p	H01L021-8242
US 6319788	B1	20011120	(200174)			H01L021-20
TW 522506	A	20030301	(200365)			H01L021-70

PRAI US 1999-460701 19991214
AB WO 200145162 A UPAB: 20031006

NOVELTY - A trench capacitor (360) is implemented in a dynamic random access memory (DRAM) (300). The trench capacitor is formed in a substrate (301). The substrate is lightly doped with p-type dopants. A p-type well (351) is provided for **isolation** of the **array** devices.
The lower portion of the trench has a width that is equal to or greater than width of the upper portion. A buried plate (365) surrounds the lower portion of the trench and serves as an electrode of the capacitor. The trench comprises a semiconductor material (320) heavily doped with dopants having a second electrical type.

DETAILED DESCRIPTION - A node dielectric layer (364) separates the electrodes of the capacitor. The node dielectric lines the inner sidewalls of the collar and the trench sidewalls in the lower portion of the trench.

USE - In a memory cell, e.g. DRAM cell of a **DRAM** or an **embedded DRAM** chip.

ADVANTAGE - Trench capacitor has reduced charge leakage and increased capacitance.

DESCRIPTION OF DRAWING(S) - The drawing shows a DRAM cell.

DRAM 300
Substrate 301
Semiconductor material 320
P-type well 351
Trench capacitor 360
Node dielectric layer 364
Buried plate 365

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L123 ANSWER 10 OF 11  WPIX  COPYRIGHT 2004 THOMSON DERWENT on STN
AN   2001-185601 [19]   WPIX
DNN  N2001-132616       DNC C2001-056201
TI   Gate formation for semiconductor with dynamic random access memory and
     logic circuit, involves doping substrate using P and N type dopants on
     partial surfaces following which annealing is performed.
IN   BRONNER, G B; DIVAKARUNI, R; MANDELMAN, J A
PA   (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
PI   JP 2000357749 A  20001226 (200119)*     11p    H01L021-8234    <--
     CN 1276623    A  20001213 (200123)             H01L021-3215
     US 6281064    B1 20010828 (200151)             H01L021-8238
     KR 2001007124 A  20010126 (200152)             H01L027-10
     SG 84601      A1 20011120 (200213)             H01L021-22
     TW 451433     A  20010821 (200239)             H01L023-02
     KR 338413     B  20020527 (200277)             H01L027-10
PRAI US 1999-325941   19990604
AB   JP2000357749 A UPAB: 20010405
     NOVELTY - Polysilicon layer (61), tungsten silicide layer (12) and nitride
     cap (13) are formed on silicon substrate (5). An insulated spacer is
     formed on the side wall of the cap, partially P and N type dopants are
     doped on different areas of the substrate and annealed to form gate
     structure.
          DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
     insulated protection cap.
          USE - Dual work function dope gate structure for
     semiconductor IC chip with dynamic random access memory (DRAM) and logic
     circuit.
          ADVANTAGE - Borderless diffusion contact can be formed reliably.
          DESCRIPTION OF DRAWING(S) - The figure shows sectional view of
     semiconductor structure.
          Silicon substrate 5
          Tungsten silicide layer 12
     Nitride cap 13
          Polysilicon layer 61
     Dwg.4/10
FS   CPI EPI
FA   AB; GI
MC   CPI: L04-C02; L04-C16
     EPI: U11-C18B5; U13-C04B1A
```

L83 ANSWER 14 OF 63 HCAPLUS
AN 2001:592225 HCAPLUS
DN 135:145768
ED Entered STN: 15 Aug 2001
TI Method for making high-aspect-ratio contacts on integrated circuits using a borderless pre-opened hard-mask technique
IN Huang, Jenn Ming
PA Taiwan Semiconductor Manufacturing Company, Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6274471	B1	20010814	US 1999-325953	19990604
				US 1999-325953	19990604

AB A method for fabricating high-aspect-ratio contacts on integrated circuits, such as **embedded DRAMs**, using a borderless pre-opened hard-mask technique is achieved. After forming **gate electrodes** for field effect transistors (FETs) and **local interconnections** from a polycide layer having a Si nitride (Si3N4) hard mask or cap layer, an anti-reflective coating was used to **protect** the FET source/drain areas. A photoresist mask and plasma etching were used to remove portions of the hard mask on the **interconnections** for contact openings, while the anti-reflective **protects** the source/drain areas. The photoresist mask and the anti-reflective coating are removed, and an interlevel dielec. (ILD) layer is deposited. The high-aspect-ratio contact openings can now be etched in the ILD layer to the source/drain areas, while concurrently etching reliable contact openings to the polycide **interconnections** where the cap Si3N4 was removed without overetching the source/drain areas.

L129 ANSWER 5 OF 8 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-229272 [24] WPIX
DNN N2001-163245 DNC C2001-068794
TI Integrated circuit chip manufacture involves activating dopant source so that P-type dopant is injected into polysilicon layers through barrier layer.
IN GAMBINO, J P; HSU, L L; MANDELMAN, J A; **RADENS, C J**; TONTI, W R
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
PI JP 2001007223 A 20010112 (200124)* 15p H01L021-8238
US 6274467 B1 20010814 (200148) H01L021-22
KR 2001007241 A 20010126 (200152) H01L027-092
TW 508752 A 20021101 (200352) H01L021-8238
PRAI US 1999-327080 19990604
AB JP2001007223 A UPAB: 20010502
NOVELTY - Gates (33,34) include gate insulating layers (24). The polysilicon layers (26,26a), barrier layer (28), dopant source (30) and capping layer (32) are formed sequentially on substrate (20). The dopant source is activated for injecting P-type dopant into polysilicon layers through barrier layer.

USE - Manufacture of integrated circuit chip.

ADVANTAGE - The double **work** function gate conductor has an insulated cap by which self alignment is performed.

DESCRIPTION OF DRAWING(S) - The figure shows manufacture of semiconductor device.

Substrate 20
Insulating layers 24
Polysilicon layers 26,26a
Barrier layer 28
Dopant source 30
Capping layer 32
Gates 33,34
Dwg.3/18
FS CPI EPI
FA AB; GI
MC CPI: L04-C02B; L04-C10B
EPI: U11-C01J2; U11-C02B2; **U11-C18A3**

L129 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:29167 HCAPLUS
DN 134:109010
ED Entered STN: 12 Jan 2001
TI Fabrication of double **work**-function semiconductor devices in manufacturing integrated circuit chips
IN Ganbino, Jeffrey Peter; Hsu, Louis L.; Mandelman, Jack Allan; **Radens, Carl J.**; Tonti, William R.
PA International Business Machines Corp., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001007223	A2	20010112	JP 2000-160941	20000530
	JP 3393846	B2	20030407		
	US 6274467	B1	20010814	US 1999-327080	19990604
	TW 508752	B	20021101	TW 2000-89107931	20000426
				US 1999-327080 A	19990604

AB The title fabrication involves forming a gate insulator film on a substrate, forming a polysilicon film on the gate insulator film, forming a carrier layer over the polysilicon layer, doping a 1st cond.-type dopant into a selected region of the polysilicon layer, providing a 2nd cond.-type dopant source on the barrier layer, forming a capping layer over the dopant source layer, patterning a gate stack, and diffusing the 2nd cond.-type dopant into the polysilicon layer through the barrier layer. The gate insulator layer may be NO or ONO film. The dopant source layer may be made from borosilicate glass TiB2, SiGeB, or B-doped polysilicon. The process provides formation of double **work** -function gate conductor having a self-aligned insulator cap in prepn. of integrated high-performance logic device/highly compact **DRAM**.
ST double **work** function semiconductor device integrated circuit
IT Memory devices
(**DRAM** (dynamic random access); fabrication of double **work**-function semiconductor devices in manufg. integrated circuit chips)
IT **Work** function
(double; fabrication of double **work**-function semiconductor devices in manufg. integrated circuit chips)
IT 7440-21-3, Silicon, properties
RL: PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(polycryst., B-doped, for boron-doping source; fabrication of double **work**-function semiconductor devices in manufg. integrated circuit chips)

L83 ANSWER 50 OF 63 WPIX
AN 2001-601204 [68] WPIX
DNN N2001-448429
TI Twin cell memory of **array** for **embedded memory** application, has **isolation** transistors located on bitlines, so that when every other bitline is isolated, adjacent bitlines are held at predetermined potential.
IN BARTH, J E; FIFIELD, J A
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 6272054 B1 20010807 (200168)* 6p G11C016-04
PRAI US 2000-702336 20001031
AB US 6272054 B UPAB: 20011121

NOVELTY - Sense amplifiers (SA1,SA2) are connected to two adjacent bitline pairs. Wordlines (W1-W4) are arranged intersecting the bitlines (B1-B8). Isolation transistors (T1,T2) are located on the bitlines such that when every other bitline of the bitlines, is being sensed, the adjacent bitlines are held at a predetermined potential by clamping transistors (C1,C2).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the method of eliminating cross talk in a twin cell memory array.

USE - For **DRAM, embedded memory** applications.

ADVANTAGE - Cross-talk between adjacent bitlines is eliminated. Twin-cell folded bitline lay out which works at lower operating voltages is realized, thereby signal and testing efficiencies are improved. Boosted array levels are eliminated for increased reliability and density. Easier integration of memory into logic technology is also realized.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of twin cell, folded bitline memory lay out.

Bitlines B1-B8
Clamping transistors C1,C2
Sense amplifiers SA1,SA2
Isolation transistors T1,T2
Wordlines W1-W4
Dwg.3/4

FS EPI

FYI Applicant 11/29/2000 priority

L83 ANSWER 52 OF 63 WPIX
AN 2001-450371 [48] WPIX
DNN N2001-333330 DNC C2001-135968
TI Formation of dynamic random access memory **array** and **support** metal oxide semiconductor field effect transistors involves saliciding tops of bitline diffusion stud landing pad in **array** and **gate conductors** for **support** transistors.
IN DIVAKARUNI, R; GRUENING, U; MANDELMAN, J A; RUPP, T S; MANDELMAN, J; RUPP, T
PA (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP

PI	US 6258659	B1	20010710	(200148)*		12p	H01L021-8242	<--
	WO 2002045130	A2	20020606	(200238)	EN		H01L000-00	
	KR 2002042420	A	20020605	(200277)			H01L027-10	
	TW 512494	A	20021201	(200353)			H01L021-8242	

PRAI US 2000-725412 20001129
AB US 6258659 B UPAB: 20010829

NOVELTY - Formation of memory **array** and **support** transistors comprises applying a block mask to **protect** **supports** while stripping nitride layer from **array** and etching exposed **polysilicon** layer to the top of gate oxide layer and to form bitline diffusion stud landing pad in **array** and **gate conductors** for the **support** transistors; and saliciding the tops of the landing pad and the **gate conductors**.

DETAILED DESCRIPTION - Formation of memory **array** and **support** transistors comprises forming a trench capacitor in a silicon substrate (11) having a gate oxide layer (18), **polysilicon** layer, and top dielectric nitride layer. A patterned mask is applied over the **array** and **support** areas. Recesses are formed in the nitride layer, **polysilicon** layer and shallow trench **isolation** region (14). A silicide and an oxide cap are formed in the recesses in the nitride layer, **polysilicon** layer and shallow trench **isolation** region. A block mask is applied to **protect** the **supports** while stripping the nitride layer from the **array**. The exposed **polysilicon** layer is etched to the top of the gate oxide layer. The nitride layer is stripped from the **support** region and a **polysilicon** layer is deposited over the **array** and **support** areas. A mask is applied to pattern and forms a bitline diffusion stud landing pad in the **array** and **gate conductors** (28) for the **support** transistors. The tops of the landing pad and the **gate conductors** are salicided. An interlevel oxide layer (36) is applied and then vias in the interlevel oxide layer are opened for establishing conductive wiring channels.

USE - For forming dynamic random access memory (DRAM) **array** and **support** metal oxide semiconductor field effect transistors (MOSFETs).

ADVANTAGE - The method fabricates very high-density **embedded**

DRAM and very high-performance **support** MOSFETs. It
provides for a bitline contact self-aligned to the active area,
eliminates boron-phosphosilicate glass reflow step, reduces
thermal budget, and allows shallower source/drains.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view
of a DRAM **array** and **support** MOSFET at a production
stage.
Silicon substrate 11
Shallow trench isolation region 14
Gate oxide layer 18
Gate conductors 28
Interlevel oxide layer 36
Dwg.18/18
TECH US 6258659 B1 UPTX: 20010829
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: A single photoresist
mask is applied to pattern both a bitline diffusion stud landing pad of
the **array** and **gate conductors** of
support transistors. Wordline conductors are formed by applying a
mid ultra violet mask to **protect** the **supports** while
partially etching the **polysilicon** layer. The tops of the landing
pad and the **gate conductors** are salicided
concurrently. A bitline contact self-aligned to the gate oxide layer is
formed by applying a block mask and etching the exposed
polysilicon layer.
FS CPI EPI
FA AB; GI
MC CPI: **L03-G04A**

L86 ANSWER 8 OF 9 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-180812 [18] WPIX
DNN N2001-128761
TI Method of manufacturing the **embedded dynamic** random access memory (DRAM) - which performs the doping process for the salicide of logic circuit after forming the DRAM area.
IN SUEN, S; SUN, S
PA (UNMI-N) UNITED MICROELECTRONICS CORP
PI TW 395053 A 20000621 (200118)* H01L027-108 <--
US 6242296 B1 20010605 (200139)# H01L021-8234 <--
PRAI TW 1998-116431 19981002; US 1998-212732 19981215
AB TW 395053 A UPAB: 20010402
NOVELTY - A method of manufacturing the **embedded dynamic** random access memory (DRAM) is disclosed, which first forms an etching stop layer after the formations of the word line and gate in the memory region and the logic circuit region, and then proceeds the memory cell array manufacturing process in the memory region. Next, the dielectric layer in the logic circuit region is removed by using the etching stop layer as the endpoint, and then the etching stop layer is removed to expose the gate. Next, a high-energy inversion channel implantation is proceeded through the gate of the logic circuit region, so as to form a source/drain region on the substrate at the side of the gate, and form a metal silicon at the source/drain region. The invention proceeds the ion-implantation after the manufacturing process of the memory cell array, which could avoid the diffusion phenomena caused by high temperature in the implantation region, and **prevent** the metal **silicon** from agglomeration at high temperature.
Dwg.0/0

L110 ANSWER 7 OF 11 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-603752 [58] WPIX
DNN N2000-446830 DNC C2000-180772
TI Dynamic random access **memory** (**DRAM**) for use in semiconductor devices includes complementary transistors in the support circuitry with **dual work**-function gates.
IN ALSMEIER, J; TOBBEN, D; TOEBBEN, D
PA (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (INFN) INFINEON NORTH AMERICA CORP

PI	EP 1039533	A2	20000927	(200058)*	EN	14p	H01L021-8242	<--
	JP 2000311991	A	20001107	(200061)		43p	H01L027-108	<--
	CN 1268772	A	20001004	(200067)			H01L027-108	<--
	US 6235574	B1	20010522	(200130)			H01L027-108	<--
	KR 2001006849	A	20010126	(200152)			H01L027-108	<--
	TW 448543	A	20010801	(200222)			H01L021-8242	<--

PRAI US 1999-273402 19990322; US 2000-568064 20000510

NOVELTY - A dynamic random access **memory** (**DRAM**) comprises complementary transistors in the support circuitry having **dual work**-function gates.

DETAILED DESCRIPTION - A dynamic random access **memory** (**DRAM**) comprises a silicon chip having a central area forming an array of **memory** cells with n-channel metal oxide semiconductor field effect transistors (N-MOSFETs), and a peripheral area forming the support circuitry including both the N-MOSFETs and p-channel metal oxide semiconductor field effect transistors (P-MOSFETs). The N-MOSFETs in the **memory** cells use N-doped polycide gates. The N- and P-MOSFETs in the support circuitry use N- and P-doped polysilicon gates.

INDEPENDENT CLAIMS are also included for:

(1) a method for forming a **DRAM** comprising (i) forming a masking layer of silicon oxide over the surface of the chip area and removing the layer from the central area where the **memory** cell arrays are to be included, but leaving it in place in the peripheral portion where the support circuitry is to be included; (ii) forming the N-MOSFETs of the **memory** cells in the central area and including N-MOSFET gate conductors (40A-B) that include an underlying polysilicon layer (14) that is doped with donor atoms and an overlying metal silicide layer; (iii) covering the chip area with a masking layer and removing it from the central area of the chip; (iv) removing the silicon oxide layer from the peripheral portion of the chip area; (v) covering the peripheral portion with a masking layer and removing it where N-MOSFETs are to be formed; (vi) forming the N-MOSFETs of the support circuitry in the peripheral portion and including N-MOSFET gate conductors as above; (vii) covering the peripheral area with a masking layer and removing it where P-MOSFETs are to be formed; and (viii) forming the P-MOSFETs of the support circuitry in the peripheral portion and including P-MOSFET gate conductors that include an underlying silicon layer that is doped with acceptor atoms and an overlying layer of a metal silicide; and

(2) a method for forming a stack that includes a monocrystalline silicon p-type substrate.

USE - For use in semiconductor devices.

ADVANTAGE - The invention provides an improved performance.
DESCRIPTION OF DRAWING(S) - The figure shows a portion of a silicon chip in a **DRAM**.
Polysilicon layer 14
Gate conductors 40A-B
Salicide source and drain contacts 56A-B, 57-59
Dwg.17/17

TECH EP 1039533 A2 UPTX: 20001114
TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The transistors in the support circuitry use salicide source and drain contacts (56A-B, 57-59) which are borderless.

FS CPI EPI

FA AB; GI

MC CPI: **L03-G04A**; L04-C14A; **L04-E01B1**
EPI: U11-C05E3; U11-C05F1; **U11-C18B5**; **U12-D02A**; **U12-Q**; **U13-C04B1A**; U13-D02A; **U14-A03B4**; **U14-C01**

L23 ANSWER 5 OF 5 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-334984 [35] WPIX
DNN N2001-241775 DNC C2001-103397
TI Silicon nitride spacer formation during fabrication of integrated circuit, involves forming semiconductor device structure on substrate, depositing silicon nitride layer on substrate, etching silicon nitride layer.
IN LEU, J; LIU, J; TSAI, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
PI US 6225203 B1 20010501 (200135)* 10p H01L021-302
PRAI US 1999-304334 19990503
AB US 6225203 B UPAB: 20010625

NOVELTY - Semiconductor device structures (S) having top and side surfaces are formed on semiconductor substrate (10). Silicon nitride layer (L) is deposited on substrate (10) and structure (S). 70-85% of layer (L) is etched using Cl2 and He. The remaining of layer (L) on top surface of structure (S) is etched using SF6, CHF3 and He to form silicon nitride spacers (40) on side surfaces of structures (S).

USE - For forming silicon nitride spacer during fabrication of integrated circuits.

ADVANTAGE - The silicon nitride spacers prevent **short** between bit lines and conducting layer within self-aligned contact (SAC) opening. The spacer of good profile and high quality, deposited by plasma-enhanced chemical vapor deposition (PE-CVD) reduce thermal budget in **embedded dynamic** random access memory (DRAM), where silicided logic circuits are protected. The spacer of good **isolation** and width, is obtained.

DESCRIPTION OF DRAWING(S) - The figure shows schematic cross sectional diagram of the silicon nitride spacer in integrated circuit.

Substrate 10

Silicon nitride spacer 40

Dwg.1/9

FS CPI EPI

L15 ANSWER 19 OF 26 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-280706 [29] WPIX
DNN N2001-200105 DNC C2001-085147
TI Simultaneous fabrication of logic devices and **embedded dynamic** random access **memory devices** by forming salicide layers on gate structures of both types of devices, but only on the source/drain region of the logic devices.
IN CHIANG, K; TZENG, K; WANG, C; YING, T
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
PI US 6207492 B1 20010327 (200129)* 10p H01L021-8242 <--
PRAI US 2000-587466 20000605
AB US 6207492 B UPAB: 20010528

NOVELTY - Logic devices and dynamic random access **memory devices** (DRAM) are simultaneously fabricated by forming a salicide layer on the gate structures and source/drain regions of the logic devices, while only forming the same salicide layer only on the gate structures of the DRAM devices.

DETAILED DESCRIPTION - Simultaneous fabrication of logic devices and **embedded DRAM** devices on a semiconductor substrate (3), includes forming first and second sets of gate structures (7-14) on an underlying gate insulator layer (5), in first and second regions of the substrate, with gate structures of the first and second sets of gate structures separated by first and second spaces, respectively. The second spaces are narrower in width than the first spaces. Lightly doped source/drain (LDD) regions (15) are formed in areas of the substrate not covered by the first or second set of gate structures. Insulator spacers (16) are formed on the sides of the gate structures. Silicon oxide blocking shapes (17b) are formed on underlying LDD regions. They are located in the second spaces in the second region of the substrate. A heavily doped source/drain region (21) is formed in an area of the first region of the substrate, not covered by the gate structures of the first set of gate structures, and not covered by the insulator spacers. A self-aligned metal silicide (salicide) layer (22) is formed on the top surface of the gate structures of the first and second sets of gate structures, and on the heavily doped regions in the first region of the substrate.

USE - For simultaneously fabricating logic devices and **embedded DRAM** devices.

ADVANTAGE - The invention presents the desired performance increase of the logic devices, offered by the salicided source/drain regions. It prevents reliability concerns for the DRAM devices by blocking the salicide formation on the DRAM source/drain regions.

DESCRIPTION OF DRAWING(S) - The figure shows a process step of fabricating logic and DRAM devices.

Substrate 3
  Gate insulator layer 5
    Polysilicon layer 6
  Gate structures 7-14
LDD regions 15
  Insulator spacers 16

Silicon oxide blocking shapes 17b
Heavily doped source/drain region 21
Salicide layer 22

Dwg.8/8

TECH US 6207492 B1 UPTX: 20010528

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The gate insulator layer is a silicon dioxide layer. The first and second sets of gate structures comprise **polysilicon** layer (6). The insulator spacers comprise silicon nitride. The silicon oxide blocking shapes comprise silicon oxide. The salicide layer is a titanium silicide, or a cobalt silicide.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The gate insulator layer is obtained via thermal oxidation procedures at a thickness of 32-150Angstrom. The gate structures of the first and second sets are obtained via low pressure chemical vapor deposition procedures at a thickness of 2000-2500Angstrom. They are doped in situ during deposition via the addition of arsine or phosphine to a silane ambient, or deposited intrinsically, then doped via implantation of arsenic or phosphorus ions at an energy of 60-120 KeV and at a dose of 1x13-1xE14 atoms/cm2. The insulator spacers are obtained via deposition of a silicon nitride layer at a thickness of 800-1000Angstrom, and defined via anisotropic reactive ion etching (RIE) procedure. The RIE procedure uses tetrafluoro methane/sulfur hexafluoride (CF4/SF6); or chlorine (Cl2) or SF6 as an etchant for silicon nitride or **polysilicon**, respectively. The silicon oxide blocking shapes are obtained via a high density plasma deposition to a thickness of 2500-3000Angstrom. They are subjected to a dry etching procedure using CF4/oxygen (O2) as an etchant, resulting in a thickness of 1000-1500Angstrom for the blocking shapes. The salicide layer is obtained via deposition of titanium or cobalt, plasma vapor deposition procedures to a thickness of 200-400Angstrom, annealing in a rapid thermal anneal furnace at 750-880degreesC to create the salicide layer on silicon or **polysilicon** features, and **removing** unreacted cobalt or titanium from the top surface of the blocking shapes and from the insulator spacers. Preferred Properties: The first spaces located between the gate structures of the first set are 4000-40000Angstrom in width. The second spaces located between the gate structures of the second set are 2250-3600Angstrom in width.

FS CPI EPI

L129 ANSWER 6 OF 8 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-226210 [23] WPIX
DNN N2001-160762 DNC C2001-067408
TI Formation of a semiconductor device involves planarizing gate stack structure using chemical mechanical polishing.
IN BRONNER, G B; GAMBINO, J P; **RADENS, C J**
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

PI	US 6200834	B1	20010313	(200123)*	7p	H01L021-335
	CN 1282103	A	20010131	(200131)		H01L021-70
	JP 2001077321	A	20010323	(200133)	7p	H01L027-10
	KR 2001015288	A	20010226	(200156)		H01L021-027
	TW 440938	A	20010616	(200203)		H01L021-28
	SG 85714	A1	20020115	(200214)		H01L021-304

PRAI US 1999-359290 19990722
IC ICM H01L021-027; H01L021-28; H01L021-3
AB US 6200834 B UPAB: 20010425

NOVELTY - A semiconductor device is formed by planarizing gate stack structure using chemical mechanical polishing.

DETAILED DESCRIPTION - Formation of a semiconductor device involves forming a substrate with a memory array region (201) and a logic device region (101). A thick gate dielectric (102) is grown on the substrate. A gate stack including a first polysilicon layer (103) is formed on the thick gate dielectric for the memory array region. The thick gate dielectric is removed on the logic device region. A thin gate dielectric is formed on the substrate over the logic device region. The layers of the gate stack in the memory array region protect the thick gate oxide during forming of the thin gate dielectric. A second polysilicon layer (300) is formed for a gate stack in the logic device region, to produce a resulting structure. A thickness of the second polysilicon layer is at least as thick as the gate stack in the memory array region. The structure is planarized using chemical mechanical polishing (CMP). The gate stacks are patterned in the memory array region and the logic device region such that a planar surface is provided during patterning of the gate stacks. Each gate stack has a planar gate stack.

USE - For forming semiconductor device.

ADVANTAGE - The method provides a planar structure for gate stack patterning. A gate cap is formed in the array (which is required for self-aligned contacts) but not in the logic regions (where the gate cap makes it more difficult to form dual **work** function gates). The logic areas are not covered by a cap nitride (e.g., silicon nitride), thus saving a mask step (e.g., a blockout mask) during implants for dual **work**-function gates. The end structure is well-planarized. The gate stacks with different thickness are achieved with good controllability. The thin and thick oxide gates can be obtained on the same chip.

DESCRIPTION OF DRAWING(S) - The figure shows processing of the logic gate stack structure.

Logic device region 101
Thick gate dielectric 102
First polysilicon layer 103

Silicides 104, 402
Pad nitride 105
Memory array region 201
Second polysilicon layer 300
Diffusions 401
Dwg.4/6

TECH US 6200834 B1 UPTX: 20010425

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The gate stack has a cap nitride layer that is used in the planarizing step as a polish stop in the memory array region. The thin gate dielectric is formed on top of the first polysilicon layer, and is used as a polish stop during CMP. Patterning is performed using lithography and reactive ion etching. The diffusions (401) and gates are doped in the logic device region by ion implantation and annealing. Silicides (104, 402) are formed on the diffusions. The gates are formed in the logic device region. The second polysilicon layer comprises an undoped polysilicon layer deposited by chemical vapor deposition. It is for the gates in the logic device region. Preferred Properties: The thick gate dielectric has a thickness of 5-50, preferably 7 nm. The first polysilicon layer has a thickness of 20-200, preferably 50 nm. The silicide comprises tungsten silicide having a thickness of 20-100, preferably 50 nm. The cap nitride has a thickness of 20-300, preferably 150 nm. The thin gate dielectric has a thickness of 2-20 nm. The thickness of the second polysilicon layer is at least as thick as the total gate stack in the memory array region. The gate stacks respectively have two different gate dielectric thickness, while maintaining a planar surface for all lithography processes and the gate stack over the thick gate dielectric is planar with the gate stack over the thin gate dielectric.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The thick gate dielectric is silicon dioxide (SiO2) or SiOxNy. The first polysilicon layer is As- and P-doped polysilicon. The silicide comprises tungsten silicide. The thin dielectric is SiO2, SiOxNy, silicon nitride, tantalum (V) oxide, or aluminum oxide. The pad nitride (105) comprises silicon nitride and functions as a polish stop.

FS CPI EPI GMPI
FA AB; GI

L83 ANSWER 47 OF 63 WPIX
AN 2002-223797 [28] WPIX
DNN N2002-171272 DNC C2002-068310
TI Manufacturing method of **embedded DRAM** by using high step coverage material to satisfy the high aspect ratio requirements.
IN HUANG, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
PI TW 426986 A 20010321 (200228)* H01L023-522
PRAI TW 1998-106463 19980427
AB TW 426986 A UPAB: 20020502
NOVELTY - DRAM manufacture uses titanium/titanium nitride (Ti/TiN) film and tungsten (W) plug to replace the traditional **poly-silicon**/tungsten silicide (WSix) as the bit-line and **local interconnection**. It also solves the issue that the WSix poorly fills in the small size contact hole by high step coverage capability tungsten thus this method is suitable for highly integrated device process.

L15 ANSWER 20 OF 26 WPIX
AN 2001-202090 [20] WPIX
DNN N2001-144113 DNC C2001-059960
TI Formation of contact nodes in semiconductor devices by creating a graded concentration of dopant by depositing first and second **polysilicon** layers, performing rapid thermal anneal, and **removing** the second **polysilicon** layer.
IN CHIANG, W; LEE, Y; WU, C; YING, T
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
PI US 6187659 B1 20010213 (200120)* 12p H01L021-4763 <--
PRAI US 1999-368861 19990806
AB US 6187659 B UPAB: 20010410

NOVELTY - Contact nodes in semiconductor devices are formed by creating a graded dopant concentration by depositing first and second **polysilicon** layers; performing Rapid Thermal Anneal; and **removing** the second **polysilicon** layer, thus partially **removing** the first **polysilicon** layer and creating an interface between lower and upper layers of the contact nodes.

DETAILED DESCRIPTION - Formation of contact nodes having lower and upper layers in semiconductor devices comprises (i) providing a semiconductor substrate; (ii) creating partially completed structures on the surface of the substrate; (iii) creating the lower layer of the contact nodes; and (iv) creating the upper layer of the contact nodes. The lower layer of the contact nodes is created by (iiia) depositing a first layer of **polysilicon** over the partially completed structure including the contact openings in the structure, (iiib) depositing a second layer of **polysilicon** over the first layer, (iiic) performing Rapid Thermal Anneal (RTA) to the first and the second layers of **polysilicon**, and (iiid) **removing** the second layer of **polysilicon**, thus partially **removing** the first layer of **polysilicon** and creating a plane of intersection between the lower and the upper layers of the contact nodes. An INDEPENDENT CLAIM is also included for a method of fabricating a logic based **embedded DRAM** on the surface of a substrate, and forming conductive plugs having an upper and a lower section to provide electrical contact between an active region in the substrate and interconnection metallization, by providing partially completed logic **embedded Dynamic** Random Access Memory (DRAM) devices on the surface of the substrate; providing the active region on the DRAM devices; creating the lower section of the conductive plugs; depositing a third layer of **polysilicon** over the surface; and patterning the third layer of **polysilicon** to form the upper section of the conductive plugs.

USE - For forming contact nodes in semiconductor devices, e.g. DRAM devices.

ADVANTAGE - The method provides contact nodes which do not degrade the device performance. The high dopant concentration at the lower layer of the nodes results in low contact resistance between the node and the substrate, and the low dopant concentration at the upper layer of the nodes results in low oxidation of the surface of the nodes.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of the contact nodes.

Gate electrodes 70, 72

Lightly doped **polysilicon** layer 80

Dwg.6d/6

TECH US 6187659 B1 UPTX: 20010410

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: Step (ii) includes forming field isolation regions to isolate the active areas from the surrounding areas of the substrate; creating a gate oxide layer on the surface of the active regions; depositing **polysilicon** layer as a single layer or in combination with conductive gate electrode material layer over the gate oxide layer; patterning and etching the **polysilicon** layer to form a gate electrode structures; forming lightly doped drain regions for source and drain regions of gate electrodes (70, 72) by light implanting of dopants; forming gate spacers on sidewalls of the structures, creating contact openings; completing the formation of source and drain regions by heavy implanting of dopants; depositing an insulation layer over the structures; and patterning and removing the insulation layer, thus creating openings which align with the contact openings between the structures. Step (iv) includes depositing and patterning a lightly doped **polysilicon** layer (80) over the plane of intersection of the lower and the upper layers of the nodes. Step (iiic) is carried out in nitric or inert gas atmosphere at 700-750degreesC for not more than 30 seconds, thus creating a graded dopant in the first layer of dielectric. The first **polysilicon** layer is lightly or heavily doped **polysilicon**.

FS CPI EPI

L83 ANSWER 54 OF 63 WPIX
AN 2001-111820 [12] WPIX
DNN N2001-082130 DNC C2001-033088
TI Reduction of aspect ratio of dynamic random access memory peripheral contact by providing a stop layer formed by a nitride layer, and etching poly layer and oxide layer in a single step.
IN DU, Y; JANG, G; SHIU, J; CHANG, C; HSU, C; TU, Y
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
PI US 6165867 A 20001226 (200112)* 10p H01L021-20
TW 410424 A 20001101 (200117) H01L021-768
PRAI TW 1998-116217 19980930
AB US 6165867 A UPAB: 20010302

NOVELTY - Aspect ratio of dynamic random access memory peripheral contact is reduced by providing a stop layer formed by a nitride layer, and simultaneously etching poly layer and oxide layer, thus the height of the peripheral contact is the same as, or lower than, a contact of a storage anode of a capacitor.

DETAILED DESCRIPTION - Reduction of aspect ratio of DRAM peripheral contact comprises forming poly layers, capacitors, a dielectric layer, and a nitride layer on a semiconductor substrate. Another poly layer is deposited on the substrate. An oxide layer is deposited and planarized to form a planar surface. A first photoresist layer is developed on predetermined locations of the oxide layer. Portions of the layers are etched away, and the first photoresist layer is removed. A second photoresist layer is developed on predetermined locations of the oxide layer. A hole, a peripheral contact, and a stacked contact are formed.

USE - For reducing aspect ratio of DRAM peripheral contact.

ADVANTAGE - Achieves good contact etching and metal deposition. It reduces the volcano effect resulted from the misalignment between stacked contacts.

DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional view of the partially accomplished semiconductor substrate.

intermediate metal layer 71

Dwg.7/7

TECH US 6165867 A UPTX: 20010302

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Properties: The thickness of the poly layers, capacitors, and silicon nitride layer formed are 500-1500 Angstrom, 4000-7000 Angstrom, and 500-1500 Angstrom, respectively. The etching selectivity for the oxide layer to the poly layer, and oxide layer to the silicon nitride layer are 8:1-15:1 and 5:1-25:1, respectively. Preferred Process: The method further comprises forming an intermediate metal layer (71) used as a **local interconnect** layer of logic device of an **embedded DRAM**.

FS CPI EPI
FA AB; GI
MC CPI: L03-G04A; L04-C06; L04-C12A; L04-C12B

L110 ANSWER 4 OF 11 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:800405 HCAPLUS
DN 133:343458
ED Entered STN: 14 Nov 2000
TI Method for forming a **DRAM** cell with a stacked capacitor
IN Kalnitsky, Alexander; Bergemont, Albert
PA National Semiconductor Corporation, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6146962	A	20001114	US 1998-40212	19980317
				US 1998-40212	19980317

AB A dynamic random-access-**memory** (**DRAM**) cell with a fin or wing-type stacked capacitor is fabricated by using a layer of polysilicon as an etch stop rather than the layer of nitride that is conventionally used. By using the layer of polysilicon, the problem of H-enhanced B diffusion in **dual work** function CMOS transistors is eliminated while at the same time increasing the capacitance of the stacked capacitor without substantially increasing the step height of the capacitor.
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; method for forming a **DRAM** cell with a stacked capacitor)

L83 ANSWER 53 OF 63 WPIX
AN 2001-233641 [24] WPIX
DNN N2001-166871
TI The manufacture method of **embedded DRAM** - with increased planarization level.
IN CHEN, J; LIN, J; TSAU, J
PA (UNMI-N) UNITED MICROELECTRONICS CORP
PI TW 409403 A 20001021 (200124)* H01L027-108
PRAI TW 1998-118337 19981104
AB TW 409403 A UPAB: 20010502

NOVELTY - This invention provides a manufacture method of **embedded DRAM**, which forms the bitline on the memory circuit region and the **local interconnect** on the logic circuit region at the same time, and could simplify the whole process. And the formation of the **local interconnect** could shorten the conductance distance, increase the device's efficiency. Besides, this invention could reduce the height difference between the logic circuit region and the memory circuit region, thus increase the planarization level of the surface.
Dwg.0/0

FS EPI
FA AB

1/9/7
DIALOG(R)File 2:INSPEC

6721979 INSPEC Abstract Number: B2000-11-2550F-043
Title: 0.42 mu m contacted pitch dual damascene copper interconnect for 0.15 mu m **EDRAM** using tapered via aligned to trench
Author(s): Hattori, T.; Masuda, H.; Sato, H.; Matsuda, T.; Yamamoto, A.; Kato, Y.; Ogawa, S.; Ohsaki, A.; Ueda, T.
Author Affiliation: ULSI Process Technol. Dev. Center, Matsushita Electron. Corp., Kyoto, Japan
Conference Title: Proceedings of the IEEE 2000 International Interconnect Technology Conference (Cat. No.00EX407) p.155-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 277 pp.
ISBN: 0 7803 6327 2 Material Identity Number: XX-2000-01452
U.S. Copyright Clearance Center Code: 0 7803 6327 2/2000/$10.00
Conference Title: Proceedings of the IEEE 2000 International Interconnect Technology Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-7 June 2000 Conference Location: Burlingame, CA,
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: A tapered via aligned to a trench without any expanding of trench width for 0.42 mu m contacted pitch dual damascene Cu interconnect has been studied. Cu via filling and via electrical properties were dependent on shapes of vias, and it has been found that the aligned tapered via has advantages for the fine pitch Cu dual damascene interconnect. (4 Refs)

1/9/8
DIALOG(R)File 2:INSPEC

6514883 INSPEC Abstract Number: B2000-04-1265D-016
Title: System on a chip' technology platform for 0.18 mu m digital, mixed signal and eDRAM applications
Author(s): Mahnkopf, R.; Allers, K.-H.; Armacost, M.; Augustin, A.; Barth, J.; Brase, G.; Busch, R.; Demm, E.; Dietz, G.; Flietner, B.; Friese, G.; Grellner, F.; Han, K.; Hannon, R.; Ho, H.; Hoinkis, M.; Holloway, K.; Hook, T.; Iyer, S.; Kim, P.; Knoblinger, G.; Lemaitre, B.; Lin, C.; Mih, R. ; Neumueller, W.; Pape, J.; Prigge, O.; Robson, N.; Rovedo, N.; Schafbauer, T.; Schiml, T.; Schruefer, K.; Srinivasan, S.; Stetter, M.; Towler, F.; Wensley, P.; Wann, C.; Wong, R.; Zoeller, R.; Chen, B.
Conference Title: International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318) p.849-52
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 943 pp.
ISBN: 0 7803 5410 9 Material Identity Number: XX-2000-00353
U.S. Copyright Clearance Center Code: 0 7803 5410 9/99/$10.00
Conference Title: International Electron Devices Meeting 1999.Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 5-8 Dec. 1999 Conference Location: Washington, DC,
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: A 0.18 mu m high performance/low power technology platform is described which allows `system on a chip integration' for a broad spectrum of products. Based on a generic digital process additional modules can be added in a modular and cost effective-manner for mixed signal as well as for eDRAM applications offering a maximum of flexibility for product designers. For mixed signal applications a precision metal-insulator-metal capacitor (MIMCAP) was developed. This is for the first time a realization of a metal-insulator-metal capacitor in a copper dual damascene metallization scheme. (3 Refs)
Subfile: B

1/9/9
DIALOG(R)File 2:INSPEC

4846995 INSPEC Abstract Number: B9502-1265D-003, C9502-5320G-002
Title: Practical test methods for verification of the **EDRAM**
Author(s): Stalnaker, K.
p.362
Publisher: Int. Test Conference, Altoona, PA, USA
Publication Date: 1994 Country of Publication: USA xii+1033 pp.
ISBN: 0 7803 2102 2
U.S. Copyright Clearance Center Code: 0 7803 2102 2/94/$4.00
Conference Title: Proceedings of International Test Conference
Conference Sponsor: IEEE Comput. Soc. Test Technol. Tech. Committee; IEEE Philadelphia Sect.; IEEE Comput. Soc.; IEEE
Conference Date: 2-6 Oct. 1994 Conference Location: Washington, DC,
Availability: IEEE Service Center, Piscataway, NJ, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The Ramtron EDRAM is a 4 Mb dynamic RAM with 2 Kb static RAM cache. It is designed for 35 ns random access times, 15 ns cache cycle times with 5 ns pulse widths and includes logic functions not found on standard DRAM's. The simple solution to testing the part is a 67 to 100 MHz machine, but a more creative solution requires the use of only slightly more creative techniques. The EDRAM, while having its own unique requirements for guaranteeing proper operation, is a part that can be fully tested an standard memory test equipment capable of 30 to 5 MHz operation with an algorithmic pattern generator. (0 Refs)
Subfile: B C
Descriptors: automatic testing; cache storage; DRAM chips; fault

L83 ANSWER 55 OF 63 WPIX
AN 2000-678674 [66] WPIX
DNN N2000-502372 DNC C2000-206316
TI Fabrication of an **embedded dynamic** random access memory comprises forming a **local interconnect** to electrically couple with a gate and a source/drain region through a contact hole.
IN CHEN, C; LIN, T; TSAO, J
PA (UNMI-N) UNITED MICROELECTRONICS CORP
PI US 6133083 A 20001017 (200066)* 7p H01L021-8234
PRAI US 1998-218543 19981222
AB US 6133083 A UPAB: 20001219

NOVELTY - Fabrication of an **embedded dynamic** random access memory comprises forming a first gate, and first and second source/drain regions in a memory circuit region; forming a second gate and a third source/drain region in a logic circuit region; forming dielectric layers over a substrate; forming contact holes, a bit line, **local interconnect**, and capacitor.

DETAILED DESCRIPTION - Fabrication of an **embedded DRAM** comprises:

(a) providing a substrate with a memory circuit region and a logic circuit region;

(b) forming a first gate, and first and second source/drain regions in the memory circuit region;

(c) forming a second gate and a third source/drain region in the logic circuit region;

(d) forming a first dielectric layer (220) over the substrate;

(e) forming a first contact hole (232) in the first dielectric layer to expose the first source/drain region (210) and a second contact hole in the same layer to expose the second gate and the third source/drain region;

(f) forming a bit line (226) to electrically couple with the first source/drain region through the first contact hole;

(g) forming a **local interconnect** (228) to electrically couple with the second gate and the third source/drain region through the second contact hole;

(h) forming a second dielectric layer (230) over the substrate;

(i) forming a third contact hole in the first and second dielectric layers to expose the second source/drain region; and

(j) forming a capacitor (234) to electrically couple with the second source/drain region through the third contact hole.

USE - For fabricating an **embedded DRAM** useful in data processing systems.

ADVANTAGE - The method is simplified since the bit line and the **local interconnect** are formed simultaneously. The conducting path of the **local interconnect** is reduced, thus improving the performance of devices. The method also decreases the elevation difference between the memory circuit region and the logic circuit region.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic,

cross-sectional diagram depicting a step in the fabrication of an **embedded DRAM**.
source/drain region 210
dielectric layers 220, 230
bit line 226
conformal barrier layer 227
local interconnect 228
contact hole 232
capacitor 234
Dwg.2C/2

TECH US 6133083 A UPTX: 20001219
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The first gate is formed by polycide. The bit line and the **local interconnect** include **polysilicon**, metal, tungsten or copper. The material used to form the conformal barrier layer is titanium, titanium nitride, tungsten nitride, tungsten-silicon-nitride, tantalum, or tantalum nitride.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: Salicides are formed on the second gate and the third source/drain region before forming the first dielectric layer. Conformal barrier layers (227) are formed in the first and second contact holes before forming the bit line and the **local interconnect**.

FS CPI EPI
FA AB; GI

L83 ANSWER 16 OF 63 HCAPLUS
AN 2000:736208 HCAPLUS
DN 133:289940
ED Entered STN: 18 Oct 2000
TI Method to fabricate **embedded dynamic** random access memory (DRAM) devices
IN Lin, Tony; Chen, Coming; Tsao, Jenn
PA United Microelectronics Corp., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6133083	A	20001017	US 1998-218543	19981222
				US 1998-218543	19981222

AB A method for fabricating an **embedded DRAM**. A substrate having a memory circuit region and a logic circuit region is provided. A 1st gate, a 1st source/drain region and a 2nd source/drain region are formed in the memory circuit region. A 2nd gate and a 3rd source/drain region are formed in the logic circuit region. A 1st dielec. layer is formed over the substrate. In the 1st dielec. layer, a 1st contact hole is formed to expose the 1st source/drain region and a 2nd contact hole is formed to expose the 2nd gate and the 3rd source/drain region. A bit line is formed to elec. couple with the 1st source/drain region through the 1st contact hole. A **local interconnect** is formed to elec. couple with the 2nd gate and the 3rd source/drain region through the 2nd contact hole. A 2nd dielec. layer is formed over the substrate. A 3rd contact hole is formed in the 1st dielec. layer and the 2nd dielec. layer to expose the 2nd source/drain region. A capacitor is formed to elec. couple with the 2nd source/drain region through the 3rd contact hole.

L91 ANSWER 13 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-542881 [49] WPIX
CR 1999-468442 [39]; 2001-307586 [32]; 2003-066252 [06]
DNN N2000-401582 DNC C2000-161478
TI Eliminating oxynitride etch residue and polysilicon **stringers**, for fabrication of two electrically isolated **memory** cells, comprises isolation of floating gates on adjacent bitlines by polysilicon oxidation.
IN CHAN, M C; EARLY, K R; TEMPLETON, M K; TRIPSAS, N H
PA (ADMI) ADVANCED MICRO DEVICES INC
PI US 6110833 A 20000829 (200049)* 17p H01L021-70
PRAI US 1998-33836 19980303

NOVELTY - Floating gates of the two memory cells are masked which are then patterned, along with the unmasked portion between, which is transformed into an insulator.

DETAILED DESCRIPTION - Fabricating first and second memory cells which are electrically isolated from one another comprises:

(i) forming a first polysilicon layer (120) on an oxide coated substrate (112);

(ii) masking this polysilicon layer to pattern floating gates of the two memory cells;

(iii) transforming the unmasked portion of the polysilicon layer into insulator by thermal oxidation; and

(iv) etching the insulator to form a gap having gradually sloping sidewalls between a floating gate of the first memory cell and a floating gate of the second cell.

An INDEPENDENT CLAIM is also included for a fabrication process which also includes: forming a sacrificial oxide layer and nitride layer (176) to form the mask; and forming an interpoly dielectric layer and a second polysilicon layer (180) substantially free of abrupt changes in step height.

USE - For semiconductor memory applications.

ADVANTAGE - Improved memory cell reliability. Poly stringers are eliminated or substantially reduced.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view illustrating a memory device after unmasked portions of second polysilicon and insulator layers are etched away.

substrate 112

first polysilicon layer 120

oxide-nitride-oxide layer 176

second polysilicon layer 180

Dwg.21/22

TECH US 6110833 A UPTX: 20001006

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - The slope of the gap is a layer of material deposited over floating gates, is preferably of oxide-nitride-oxide (ONO) with substantially uniform thickness after deposition over the floating gates and gap.

FS CPI EPI
FA AB; GI

L91 ANSWER 2 OF 28 HCAPLUS

AN 2000:606838 HCAPLUS

DN 133:186545

ED Entered STN: 31 Aug 2000

TI Elimination of oxide/nitride/oxide etch residue and polysilicon **stringers** through isolation of floating gates on adjacent bitlines by polysilicon oxidation in semiconductor **memory** device fabrication

IN Early, Kathleen R.; Templeton, Michael K.; Tripsas, Nicholas H.; Chan, Maria C.

PA Advanced Micro Devices, Inc., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110833	A	20000829	US 1998-33836	19980303
	US 6455888	B1	20020924	US 2000-506298	20000217

AB A method for fabricating a 1st memory cell and a 2nd memory cell elec. isolated from each other is provided. A 1st polysilicon (poly I) layer is formed on an oxide coated substrate. Then, a sacrificial oxide layer and nitride layer are formed for masking the poly I layer. At least a portion of the masking layer is etched to pattern the 1st memory cell and the 2nd memory cell and an unmasked portion there between. The unmasked portion of the poly I layer is transformed into an insulator via thermal oxidn. such that the insulator separates a floating gate of the 1st memory cell from a floating gate of the 2nd memory cell. The insulator is etched so as to form a gap having gradually sloping sidewalls between a floating gate of the 1st memory cell and a floating gate of the 2nd memory cell, the gap isolating the floating gate of the 1st memory cell from the floating gate of the 2nd memory cell. Thereafter, an inter-poly dielec. layer and a 2nd polysilicon (poly II) layer are formed substantially free of abrupt changes in step height.

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes 106957-70-4, Silicon oxide (SiO1-2)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(elimination of oxide/nitride/oxide etch residue and polysilicon stringers through isolation of floating gates on adjacent bitlines by polysilicon oxidn. in semiconductor memory device fabrication)

L86 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:69412 HCAPLUS
DN 132:188276
ED Entered STN: 30 Jan 2000
TI Effects of Ti-capping on formation and stability of Co silicide I. Solid phase reaction of Ti to Co/Si system
AU Sohn, Dong Kyun; Park, Ji-Soo; Park, Jin Won
CS Research and Development Division, Hyundai MicroElectronics Company Limited, Cheongju-si, 361-480, S. Korea
SO Journal of the Electrochemical Society (2000), 147(1), 373-380
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 66
AB We have investigated the formation and thermal stability of Co silicide on Si using a Ti-cap. We propose that Ti retards the reaction between Co and the **Si** substrate and also **prevents** oxygen contamination. The Ti-capped CoSi2 has a higher transformation temp. and thinner film thickness than TiN-capped CoSi2. A 15 nm thick Ti-cap provides a CoSi2 layer with a more uniform interface and higher thermal stability compared to CoSi2 layers with a TiN-cap. The increased uniformity of the silicide/Si interface results from the retarded Co-Si reaction, due to the formation of a CoTi binary phase. The high thermal stability can be explained by a Ti-stuffing model. From anal. of the depth profile, it is likely that surface Ti diffuses rapidly into the CoSi2 grain boundaries and slows the agglomeration process, thereby increasing the thermal stability. As a result, Ti-capped Co silicide formed on a 0.15 .mu.m wide polycryst. Si gate shows thermal budget limit as high as 900.degree.C for 30 min. Based on the results of capacitance-voltage and time-dependent dielec. breakdown measurements, we can conclude that Ti-capped Co silicide is a candidate as a gate electrode for high thermal budget devices such as logic with **embedded dynamic** random access memory.

20/9/11

DIALOG(R)File 2:INSPEC

6715328 INSPEC Abstract Number: B2000-11-2570D-003

Title: A fabrication method for high performance embedded DRAM of 0.18 mu m generation and beyond

Author(s): Yoshida, T.; Takato, H.; Sakurai, T.; Kokubun, K.; Hiyama, K.; Nomachi, A.; Takasu, Y.; Kishida, M.; Ohtsuka, H.; Naruse, H.; Morimasa, Y. ; Yanagiya, N.; Hashimoto, T.; Noguchi, T.; Miyamae, T.; Iwabuchi, N.; Tanaka, M.; Kumagai, J.; Ishiuchi, H.

Author Affiliation: ULSI Device Eng. Lab., Toshiba Corp., Yokohama, Japan

Conference Title: Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044) p.61-4

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA 596 pp.

ISBN: 0 7803 5809 0 Material Identity Number: XX-2000-01396

U.S. Copyright Clearance Center Code: 0 7803 5809 0/2000/$10.00

Conference Title: Proceedings of the IEEE 2000 Custom Integrated Circuits Conference

Conference Sponsor: IEEE Solid State Circuits Soc

Conference Date: 21-24 May 2000 Conference Location: Orlando, FL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: A new fabrication method for **embedded DRAM** of 0.18 mu m generation is proposed, which realizes full compatibility with logic process such as Co salicide, **dual work** function **gate**, small thermal budget and metalization, and introduces Self-aligned Salicide Block (SSB), a new process technology. Fabricated **embedded DRAM** shows excellent characteristics with respect to both retention time and MOSFET AC/DC performance, promising high performance of SOC (System On a Chip) applications. (1 Refs)

Subfile: B

Descriptors: application specific integrated circuits; CMOS memory circuits; **DRAM** chips; integrated circuit technology; random-access storage

L83 ANSWER 6 OF 63 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:744894 HCAPLUS
ED Entered STN: 23 Sep 2003
TI The manufacture method of **embedded dram**
IN Lin, Jian-Ting; Chen, Jin-Lai; Tsau, Jen
PA United Microelectronics Corp., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 409403	B	20001021	TW 1998-87118337	19981104
				TW 1998-87118337	19981104

AB This invention provides a manuf. method of **embedded DRAM**, which forms the bitline on the memory circuit region and the **local interconnect** on the logic circuit region at the same time, and could simplify the whole process. And the formation of the **local interconnect** could shorten the conductance distance, increase the device's efficiency. Besides, this invention could reduce the height difference between the logic circuit region and the memory circuit region, thus increase the planarization level of the surface.

L15 ANSWER 21 OF 26 WPIX
AN 2000-627548 [60] WPIX
DNN N2000-464894 DNC C2000-187966
TI Fabrication of dual gate structure of **embedded DRAM** by forming **poly-silicon** spacer and silicon nitride spacer.
IN SUN, S
PA (UNMI-N) UNITED MICROELECTRONICS CORP

PI	TW 386290	A	20000401 (200060)*	18p	H01L021-8242	<--
	US 6153459	A	20001128 (200102)#		H01L021-8244	<--

PRAI TW 1998-113549 19980818; US 1998-192643 19981116

AB TW 386290 A UPAB: 20001214
NOVELTY - A fabrication method of dual gate structure of **embedded DRAM**. First, form 1st **poly silicon**, silicide and silicon nitride layers upon the substrate. Then define the silicon nitride, tungsten silicide and **poly silicon** layers to get a gate structure and remove these three layers at logic circuit area simultaneously. Next, form 2nd **poly silicon** layer and make a dual-gate structure at logic circuit area and then a **poly silicon** spacer is simultaneously formed at the sidewall of the gate structure at memory area. **Remove** the **poly silicon** spacer and form silicon nitride spacers at gate and dual-gate structures. Finally, make metal silicide on the dual-gate structure and exposed substrate of logic circuit area.

USE - Fabrication of dual gate structure of **embedded DRAM** by forming **poly-silicon** spacer and silicon nitride spacer.

L15 ANSWER 3 OF 26 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:830354 HCAPLUS
DN 133:358262
ED Entered STN: 28 Nov 2000
TI Method of fabricating the dual gate structure of **embedded DRAM**
IN Sun, Shih-Wei
PA United Microelectronics Corp., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6153459	A	20001128	US 1998-192643	19981116
PRAI	US 1998-192643		19981116		

AB A method of fabricating a dual gate of **embedded DRAM** forms a conductive layer on a substrate having a memory cell region and a logic circuitry. A gate structure is then formed on the substrate of the memory cell region and the conductive layer of the logic circuitry is removed by patterning the conductive layer. A **polysilicon** layer is then deposited and a dual gate structure is formed by patterning the **polysilicon** layer, and simultaneously, a **polysilicon** spacer is formed on the sidewall of the gate structure in the logic circuitry. The **polysilicon** spacer is then **removed**. An insulated spacer is formed on the sidewall of the gate structure and the dual gate structure, and a silicide layer is formed on the dual gate structure and the exposed substrate of the logic circuitry.

IT **7440-21-3**, **Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**polycryst.**; method of fabricating the dual gate structure of **embedded DRAM**)

20/9/12
DIALOG(R)File 2:INSPEC

6693531 INSPEC Abstract Number: B2000-10-1265D-013, C2000-10-5320G-008
Title: High-performance embedded SOI DRAM architecture for the low-power supply
Author(s): Yamauchi, T.; Morisita, F.; Maeda, S.; Arimoto, K.; Fujishima, K.; Ozaki, H.; Yoshihara, T.
Author Affiliation: ULSI Dev. Center, Mitsubishi Electr. Corp., Hyogo, Japan
Journal: IEEE Journal of Solid-State Circuits vol.35, no.8 p. 1169-78
Publisher: IEEE,
Publication Date: Aug. 2000 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
SICI: 0018-9200(200008)35:8L.1169:HPED;1-5
Material Identity Number: I022-2000-008
U.S. Copyright Clearance Center Code: 0018-9200/2000/$10.00
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: This paper presents the high-performance **DRAM array** and logic architecture for a sub-1.2-V **embedded** silicon-on-**insulator** (SOI) **DRAM** . The degradation of the transistor performance caused by boosted wordline voltage level is distinctly apparent in the low voltage range. In our proposed stressless SOI **DRAM array** , the applied electric field to the gate oxide of the memory-cell transistor can he relaxed. The crucial problem that the gate oxide of the **embedded-DRAM** process must be thicker than that of the logic process can be solved. As a result, the performance degradation of the logic transistor can be avoided without forming the gate oxides of the **memory-cell array** and the logic **circuits** individually. In addition, the data retention characteristics can be improved. Secondly, we propose the body-bias-controlled SOI-**circuit** architecture which enhances the performance of the logic **circuit** at sub-1.2-V power supply voltage, Experimental results verify that the proposed **circuit** architecture has the potential to reduce the gate-delay time up to 30% compared to the conventional one. This proposed architecture could provide high performance in the low-voltage **embedded** SOI **DRAM**. (13 Refs)
Subfile: B C

20/9/16
DIALOG(R)File 2:INSPEC

6506886 INSPEC Abstract Number: B2000-03-2570D-076
Title: Thermally robust **dual-gate** CMOS integration technologies for high-performance **DRAM-embedded** ASICs
Author(s): Togo, M.; Mogami, T.; Kubota, R.; Nobusawa, H.; Hamada, M.; Inoue, K.; Mikagi, K.; Yoshida, K.; Soda, E.; Kishi, S.; Satou, K.; Yamamoto, T.; Takeda, K.; Aimoto, Y.; Nakazawa, Y.; Toyoshima, H.
Author Affiliation: Silicon Syst. Res. Labs., NEC Corp., Sagamihara, Japan
Conference Title: International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318) p.49-52
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 943 pp.
ISBN: 0 7803 5410 9 Material Identity Number: XX-2000-00353
U.S. Copyright Clearance Center Code: 0 7803 5410 9/99/$10.00
Conference Title: International Electron Devices Meeting 1999. Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 5-8 Dec. 1999 Conference Location: Washington, DC,
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: We have demonstrated three key integration technologies of thermally stable **dual-gate** CMOSFETs for **DRAM-embedded** ASICs. These technologies include: (1) a thermally stable W-polycide gate for every MOSFET and CoSi/sub 2/ diffusion for logic CMOS to maintain low resistance, (2) nitrogen implantation into WSi/sub 2/ to prevent lateral dopant diffusion without gate depletion, and (3) a Si/sub 3/N/sub 4//TEOS-BPSG stacked interlayer for self-aligned contacts (SAC) without boron penetration in PMOSFETs. High-performance CMOSFETs using these technologies and 5 metal layers result in a flexible circuit design which can achieve 6.8 ns access speed in a 64 Mb **DRAM-embedded** macro with a 0.25 mu m design rule. (5 Refs)

20/9/17

DIALOG(R)File 2:INSPEC

6490140 INSPEC Abstract Number: B2000-03-1265F-017, C2000-03-5130-015

Title: New **embedded DRAM** technology using self-aligned salicide block (SSB) process for 0.18 mu m SOC (system on a chip)

Author(s): Kokubun, K.; Takato, H.; Sakurai, T.; Koike, H.; Nomachi, A.; Ohtsuka, H.; Harakawa, H.; Sato, W.; Tanaka, M.; Naruse, H.; Kamijo, H.; Kumagai, J.; Ishiuchi, H.

Author Affiliation: ULSI Device Eng. Lab., Toshiba Corp., Yokohama, Japan

Conference Title: 1999 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.99CH36325) p.155-6

Publisher: Japan Soc. Appl. Phys, Tokyo, Japan

Publication Date: 1999 Country of Publication: Japan xvi+174 pp.

ISBN: 4 930813 93 X Material Identity Number: XX-1999-02839

Conference Title: 1999 Symposium on VLSI Technology. Digest of Technical Papers

Conference Date: 14-16 June 1999 Conference Location: Kyoto, Japan

Language: English Document Type: Conference Paper (PA)

Treatment: New Developments (N); Practical (P); Experimental (X)

Abstract: New **embedded DRAM** technology for 0.18 mu m SOC (system on a chip) using the self-aligned salicide block (SSB) process is proposed. This process technology provides full process compatibility with high performance logic and minimum number of process steps, resulting in low process cost and short TAT (turnaround time). We fabricated a **DRAM** array macro using this technology with Co salicide, **dual work** function **gate** and aluminum bitline processes, and confirmed excellent **DRAM** retention characteristics by using a negative wordline bias scheme. (4 Refs)

Subfile: B C

Descriptors: **DRAM** chips; **embedded** systems; integrated circuit interconnections; integrated circuit metallisation; integrated circuit reliability; integrated logic circuits; microprocessor chips; **work function**

20/9/18

DIALOG(R)File 2:INSPEC

6284391 INSPEC Abstract Number: B1999-08-2570D-003

Title: Merged DRAM with Logic/Analog (MDLA) technology for single-chip solution

Author(s): Jong Shik Yoon; Sunil Yu; Hyae Ryoung Lee; Chul-Soon Kwon; Dong Woo Kim; Won Chul Kim; Chang-Sik Choi

Author Affiliation: LSI TD, Samsung Electron. Co. Ltd., Kyungki, South Korea

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.38, no.4B p.2183-7

Publisher: Publication Office, Japanese Journal Appl. Phys,

Publication Date: April 1999 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

SICI: 0021-4922(199904)38:4BL.2183:MDWL;1-L

Material Identity Number: F221-1999-010

Conference Title: Proceedings of the 1998 International Conference on Solid State Devices and Materials (SSDM'98)

Conference Date: 7-10 Sept. 1998 Conference Location: Hiroshima, Japan

Language: English Document Type: Conference Paper (PA); Journal Paper

Treatment: Practical (P); Experimental (X)

Abstract: This paper describes a process integration of Merged DRAM (dynamic random access memory) with Logic and Analog (MDLA) using high performance 0.35 mu m CMOS technology for the implementation of "System on a Chip". DRAM whose cell size was 2.1 mu m/sup 2/ and analog cores were **embedded** in 0.35 mu m logic chip without sacrifice of transistor performance of logic circuitry. The obtained values of I/sub dsaturation/ of NMOS/PMOS transistors were about 530 and 250 mu A/ mu m at 3.3 V, respectively. **Dual gate** oxide process was developed to support 5 V operation as well as 3.3 V operation. The key process feature of this study was that the aluminum alloy layer was used as a bit line in DRAM cells on the contrary to the employment of polycide in the conventional DRAM technology. In this study, metal-**insulator**-metal (MIM) capacitor scheme was employed for the applications in high-resolution analog cores. The low value of voltage coefficient of capacitance as low as 10 ppm/V could be achieved with MIM scheme. (5 Refs)

Subfile: B

Descriptors: CMOS analogue integrated circuits; CMOS logic circuits; CMOS memory circuits; **DRAM chips**; integrated circuit technology

L110 ANSWER 8 OF 11 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1999-421724 [36] WPIX
DNN N1999-315158 DNC C1999-123980
TI Forming a dual gate dielectric **dual work** function integrated circuit.
IN BRONNER, G B; EL-KAREH, B; SCHUSTER, S E
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

PI	EP 935285	A1	19990811	(199936)*	EN	16p	H01L021-8239	
	CN 1225507	A	19990811	(199950)			H01L021-8234	<--
	JP 11317459	A	19991116	(200005)		10p	H01L021-8234	<--
	SG 70150	A1	20000125	(200015)			H01L021-8242	<--
	TW 368734	A	19990901	(200034)			H01L021-8242	<--
	US 6087225	A	20000711	(200037)			H01L021-8234	<--
	KR 99072249	A	19990927	(200048)			H01L021-8232	
	KR 331527	B	20020406	(200267)			H01L021-8232	

PRAI US 1998-18939 19980205
AB EP 935285 A UPAB: 19990908

NOVELTY - A dual gate dielectric IC is formed by forming a gate stack over a first dielectric layer, removing part of the stack to re-expose the substrate and forming a second dielectric layer of different thickness on the re-exposed substrate.

DETAILED DESCRIPTION - An integrated circuit chip is formed by:

(i) patterning a gate stack including a first dielectric layer on a wafer;

(ii) adding a second dielectric layer on the wafer of different thickness from the first;

(iii) adding a first gate on the second dielectric layer;

(iv) removing portions of the gate stack to define a second gate structure; and

(v) forming conduction regions adjacent each gate.

Preferably the dielectric layers are oxide and the gates are poly silicon.

USE - Especially as a dual gate oxide, **dual work** function CMOSFET for a **DRAM** logic device.

ADVANTAGE - Two gate oxide thickness are formed on the same chip using a simple process.

DESCRIPTION OF DRAWING(S) - The drawing shows thick and thin oxide FET structures on the same wafer formed by the method of the invention

Thick gate oxide 104
Thin gate oxide 116
Thick oxide poly silicon gate stack 128
Thin oxide poly silicon gate 120

Dwg.6/9

FS CPI EPI
FA AB; GI
MC CPI: **L03-G04A; L04-E01B1**
EPI: U11-C02J6; U11-C05B9B; U11-C05F1

L110 ANSWER 5 OF 11 HCAPLUS

AN 1999:519624 HCAPLUS

DN 131:137939

ED Entered STN: 19 Aug 1999

TI Fabrication of integrated circuits having dual-gate-oxide **dual-work**-function CMOS devices

IN Bronner, Gary Bela; El-Kareh, Badih; Schuster, Stanley Everett

PA International Business Machines Corporation, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 935285	A1	19990811	EP 1999-300234	19990114
	US 6087225	A	20000711	US 1998-18939	19980205
	CN 1225507	A	19990811	CN 1999-100913	19990104
	JP 11317459	A2	19991116	JP 1999-21159	19990129
	JP 3111059	B2	20001120		
				US 1998-18939 A	19980205

AB A method of forming integrated circuit chips including 2 dissimilar type NFETs and/or 2 dissimilar type PFETs on the same chip, such as both thick- and thin-gate- oxide FETs, is described. A **DRAM** array may be constructed of the thick-oxide FETs and logic circuits may be constructed of the thin-oxide FETs on the same chip. First, a gate stack including a 1st, thick gate SiO2 layer is formed on a wafer. The stack includes a doped polysilicon layer on the gate oxide layer, a silicide layer on the polysilicon layer, and a nitride layer on the silicide layer. Part of the stack is selectively removed to re-expose the wafer where logic circuits are to be formed. A thinner gate oxide layer is formed on the re-exposed wafer. Next, gates are formed on the thinner gate oxide layer and thin oxide NFETs and PFETs are formed at the gates. After selectively siliciding thin oxide device regions, gates are etched from the stack in the thick oxide device regions. Finally, source and drain regions are implanted and diffused for the thick gate oxide devices.

IT **Memory** devices
(**DRAM** (dynamic random access); fabrication of integrated circuits having dual-gate-oxide **dual-work**-function CMOS devices for)

IT MOS devices
(complementary; fabrication of integrated circuits having dual-gate-oxide **dual-work**-function CMOS devices)

IT Etching
Ion implantation
Siliconizing

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; fabrication of integrated circuits having dual-gate-oxide **dual-work**-function CMOS devices contg.)

L15 ANSWER 23 OF 26 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-410863 [35] WPIX
DNN N2000-307085 DNC C2000-124435
TI Manufacture of an **embedded dynamic** random access memory for use inside high volume processing circuits e.g. graphic processor requires only two critical and non-critical mask patterns to pattern out the memory gates and logic gates.
IN LIAU, K; LIAO, K
PA (UNMI-N) UNITED MICROELECTRONICS CORP; (UNSI-N) UNITED SILICON INC
PI US 6069037 A 20000530 (200035)* 10p H01L021-8242 <--
TW 428311 A 20010401 (200156) H01L027-108 <--
PRAI TW 1998-113976 19980825

NOVELTY - An **embedded dynamic** random access memory (DRAM) is made requiring only two mask patterns to pattern out the DRAM gates and logic gates. Only one of the masks is critical requiring precise dimensions.

DETAILED DESCRIPTION - Manufacture of an **embedded DRAM** comprises providing a semiconductor substrate (200) including DRAM (201a) and logic (201b) circuit regions, having a field oxide layer (204) and a gate oxide layer (202). A **polysilicon** layer (206) and an etching barrier layer are then formed over the semiconductor substrate which are then removed together with the gate oxide layer above the memory circuit region. A second gate region oxide layer is formed over the substrate in the memory circuit region and a second **polysilicon** layer (214a), a tungsten silicide layer (216a), and a silicon nitride layer (218a) are formed above the second gate oxide layer and the etching barrier layer. Memory and logic gate patterns are formed over the substrate structure. A portion of the silicon nitride layer, the tungsten silicide layer, and the second **polysilicon** layer are then **removed** to expose the etching barrier in the logic circuit region and the second gate oxide layer in the memory circuit region forming a memory gate structure. A portion of the etching barrier layer and the first **polysilicon** layer are then **removed** to expose the first gate oxide layer using the silicon nitride layer, tungsten silicide layer, and the second **polysilicon** layer above the logic circuit region as a hard mask and then removing the etching barrier layer. Spacers are then formed on the sidewall of the first **polysilicon** layer and the memory gate structure. Source/drain regions are formed in the substrate on each side of the memory gate structure and on each side of the first **polysilicon** layer. A self-aligned silicide layer (228a) over the first **polysilicon** layer and the second source/drain regions are then formed to constitute a logic gate.

USE - For making dynamic random access memory (DRAM) for use inside high volume processing circuits e.g. graphic processor.

ADVANTAGE - Complexity of the manufacturing operation is lowered, thus, saving production costs.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic, cross-sectional view in producing an **embedded DRAM**.

Semiconductor substrate 200

DRAM circuit region 201a
Logic circuit 201b
Gate oxide layer 202
Field oxide layer 204
First **polysilicon** layer 206
Second **polysilicon** layer 214a
Tungsten silicide layer 216a
Silicon nitride layer 218a
Self-aligned silicide layer 228a

Dwg.2I/2

TECH US 6069037 A UPTX: 20000725
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Property: The first and second **polysilicon** layers is 2000Angstrom and 1000Angstrom thick, respectively. The etching barrier is 300Angstrom thick. The tungsten silicide layer is 1000Angstrom thick. And the silicon nitride layer is 1000Angstrom thick.

ABEX US 6069037 A UPTX: 20000725
EXAMPLE - In an EMBODIMENT of the method, forming the etching barrier includes depositing silicon nitride layer and etching the barrier layer includes depositing silicon dioxide layer. Forming the self-aligned silicide layer includes reacting silicon with titanium to form a titanium silicide layer, and silicon with cobalt to form cobalt silicide layer. Forming the first and second source/drain regions includes implanting ions to form a lightly doped region. The barrier and the first polysilicon layer are etched using the hard mask, which is then removed after etching.

FS CPI EPI

FA AB; GI

MC CPI: L03-G04A; L04-C10F

L112 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:539631 HCAPLUS
DN 133:259950
ED Entered STN: 07 Aug 2000
TI A cost effective **embedded DRAM** integration for high-density memory and high performance logic using 0.15-.mu.m technology node and beyond
AU Ha, Daewon; Shin, Dongwon; Koh, Gwan-Hyeob; Lee, Jaegu; Lee, Sanghyeon; Ahn, Yong-Seok; Jeong, Hongsik; Chung, Taeyoung; Kim, Kinam
CS Technology Development, Samsung Electronics Company, Kyungki, 449-900, S. Korea
SO IEEE Transactions on Electron Devices (2000), 47(7), 1499-1506
CODEN: IETDAI; ISSN: 0018-9383
AB In this paper, a 0.15-.mu.m **embedded DRAM** technol. is described which provides a cost-effective means of delivering high bandwidth, low power consumption, noise immunity, and a small foot print chip. The key technologies for high-performance transistors are dual thickness gate oxide, dual **work-function** gate with Si3N4 capped Ti polycide, and selective Co silicidation of source/drain diffusion by Si3N4 liner. In order to increase the memory cell efficiency, all memory cell contacts in DRAM arrays are formed by self-aligned contact (SAC) etching. A low-temp. Al2O3 stacked cell capacitor with hemispherical grain (HSG) makes it possible to realize the sufficient storage capacitance in DRAM arrays and the high performance transistor. CMP planarization of interlayer dielec. enlarges the depth of focus for lithog. and enables the multilevel metalization. These integration technologies can be fairly extendible to the future **embedded DRAM** in the 0.13-.mu.m technol. node and beyond.
IT **Memory devices**
(DRAM (dynamic random access); cost effective **embedded DRAM** integration for high-d. memory and high-performance logic using 0.15-.mu.m technol.)
IT Integrated circuits
Memory devices
(cost effective **embedded DRAM** integration for high-d. memory and high-performance logic using 0.15-.mu.m technol.)

L15 ANSWER 26 OF 26 JAPIO (C) 2004 JPO on STN
AN 1999-330417 JAPIO
TI METHOD FOR ASSEMBLING **EMBEDDED DRAM** DEVICE AND THE **EMBEDDED DRAM** DEVICE HAVING DUAL GATE CMOS STRUCTURE
IN RIN EISHO
PA UNITED MICROELECTRONICS CORP
PI JP 11330417 A 19991130 Heisei
AI JP 1998-208053 (JP10208053 Heisei) 19980723
PRAI TW 1998-107281 19980512
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
IC ICM **H01L027-108**
ICS **H01L021-8242; H01L027-10**
AB PROBLEM TO BE SOLVED: To prevent a shallow PN junction between a source/drain region and a substrate from being made still thinner by a self-aligned silicide process.
SOLUTION: An SEG process is carried out for forming plural amorphous **silicon** layers on **polycrystalline silicon** for various FETs and source/drain regions. A self-aligned silicide process is carried out on the layers to form titanium silicide layers 344, 346, 348 and 350, and the titanium silicide layers 344, 346, 348 and 350 are spaced from the substrate by source/drain regions. Since the formation of the titanium silicide layers 344, 346, 348 and 350 does not deplete the silicon atoms part of a substrate 300, shallow junctions causing leakage current in a DRAM device are prevented from being still thinner. In the case of a dual gate complementary metal oxide semiconductor(CMOS) structure, since the silicide layers are formed after the activation of impurities in the source/drain regions generation of mutual diffusion effect between an N-type **polycrystalline silicon** layer and a P-type **polycrystal silicon** layer can be **prevented**.

L110 ANSWER 11 OF 11 JAPIO (C) 2004 JPO on STN
AN 1999-317459 JAPIO
TI MANUFACTURE OF DUAL-GATE OXIDE **DUAL WORK** FUNCTION CMOS
IN BRONNER GARY BELA; EL-KAREH BADIH; SCHUSTER STANLEY EVERETT
PA INTERNATL BUSINESS MACH CORP <IBM>
PI JP 11317459 A 19991116 Heisei
AI JP 1999-21159 (JP11021159 Heisei) 19990129
PRAI US 1998-18939 19980205
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
IC ICM **H01L021-8234**
ICS H01L027-088; H01L027-10; **H01L027-108**; **H01L021-8242**

AB PROBLEM TO BE SOLVED: To provide a manufacturing method for a dual-gate oxide which is capable of manufacturing a single integrated circuit chip, wherein a logic circuit and a **DRAM** are combined and manufacturing a field effect transistor(FET) having a **dual work** function.

SOLUTION: First, a thick gate oxide layer 104 is formed on a wafer, than a doped polysilicon layer 106, a silicide tungsten layer 108 and a nitride layer 110 are successively laminated on the oxide layer in order to form a gate stack. A part of the stack is selectively removed, and the wafer on which the logic circuits are formed in re-exposed. A thin gate oxide layer 116 is formed on the re-exposed region of the wafer, a polysilicon gate 120 is formed thereon, and a thick oxide NFET and PFET are formed on the gate. A thick oxide device region is selectively changed into a silicide 146, then the gate is etched from the stack in the thick oxide device region. Finally, dopant ions are implanted into source/drain regions 140 and 142 of the thick gate oxide device and are made to diffuse, and a deep junction and a **dual work** function gate are formed.

L104 ANSWER 2 OF 2 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-398756 [34] WPIX
DNN N2000-298642
TI Limited-voltage bit line **isolation** circuit - as a **support** circuit for selectively **isolating** or connecting the **DRAM** cell in the **DRAM array**.
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
PI TW 368655 A 19990901 (200034)* G11C011-34
PRAI TW 1998-107276 19980512
AB TW 368655 A UPAB: 20000725
The invention relates to a kind of limited-voltage isolation circuit used for the bit-line pairs in branches of dynamic random access **memory** cells. The limited-voltage bit line isolation circuit will selectively connect or disconnect the original bit-line and complement bit-line of the **DRAM** to the latched sensing amplifier and the original bit-line and complement bit-line of the pre-charged equalizer. The limited-voltage bit-line isolation circuit comprises two linked groups of N-type MOS transistors and one P-type MOS transistor and allocated on the original bit-line and complementary bit-line. The isolated voltage control circuit provides the gate voltage of N-type and P-type MOS transistors in order to activate or deactivate the limited-voltage isolation control circuit. During the reading cycle, to latch the sensing amplifier and to sense and amplify the charges of selected cells and begin to drive the first and second part of original bit-line and complementary bit-line to the power supply voltage or grounding level. When the voltage level of the first and second part original bit-line and complementary bit-line close to the threshold voltage of a MOS transistor, the limited-voltage bit-line isolation circuit will not be activated. The first part of the original bit-line and complementary bit-line will oscillate to the lower voltage level so as to reduce the noise coupled to the neighbored bit-line.
FS EPI
FA AB
MC EPI: **U13-C04B1A**; **U14-A03B4**; U14-A07A

L110 ANSWER 9 OF 11 WPIX

AN 1999-373734 [32] WPIX
DNN N1999-279038 DNC C1999-110442
TI Process provides **dual work** function doping.
IN BRONNER, G B; GAMBINO, J P; MANDELMAN, J A; RADENS, C J; TONTI, W R; TONTI, W R P
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

PI								
EP 929101	A1	19990714	(199932)*	EN	10p	H01L021-8234	<--
US 5937289	A	19990810	(199938)			H01L021-8238	
CN 1223464	A	19990721	(199947)			H01L021-3215	
JP 11260935	A	19990924	(199951)		8p	H01L021-8234	<--
SG 70142	A1	20000125	(200015)			H01L021-28	
KR 99067774	A	19990825	(200046)			H01L021-334	
KR 303410	B	20010926	(200233)			H01L021-334	
TW 464956	A	20011121	(200248)			H01L021-265	

PRAI US 1998-3106 19980106

NOVELTY - A process providing **dual work** function doping comprises forming gate structures comprising gate conductor (3) between two insulating layers (2,4) and doping the structures with dopants of differing conductivity type using sidewall doping.

DETAILED DESCRIPTION - A process giving **dual work** function doping comprises depositing sequentially on a semiconductor substrate (1) layers of insulator (2), gate conductor (3) and second insulator (4) and delineating to form gates with the second insulator self-aligned on top of the gate. Some gates are then doped through a sidewall with dopant of first conductivity and the others with dopant of second conductivity.

An INDEPENDENT CLAIM is also included for an array of gate structures as above.

USE - In providing **dual work** functions (claimed), especially for **DRAMs** and logic circuits

ADVANTAGE - Either P+ or N+ doping is selectively applied, while a self-aligned gate cap is created at the same time.

DESCRIPTION OF DRAWING(S) - A cross-section of the gate structures is shown.

Substrate 1
Insulating layers 2,4
Gate conductor 3
Dwg.5/8

TECH EP 929101 A1 UPTX: 19990813
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - The gate conductor is P-doped polysilicon and N-doped silicate glass is provided on sidewalls of gate to be N-doped and diffusion brought about.

FS CPI EPI
FA AB; GI

L129 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:457970 HCAPLUS
DN 131:81570
ED Entered STN: 27 Jul 1999
TI Providing dual **work** function doping of gate structures
IN Bronner, Gary Bela; Gambino, Jeffrey P.; Mandelman, Jack A.; **Radens, Carl J.**; Tonti, William Robert
PA International Business Machines Corporation, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 929101	A1	19990714	EP 1998-310525	19981221
	US 5937289	A	19990810	US 1998-3106	19980106
	CN 1223464	A	19990721	CN 1998-122391	19981204
	CN 1113402	B	20030702		
	SG 70142	A1	20000125	SG 1998-5847	19981216
	JP 11260935	A2	19990924	JP 1999-47	19990104
	JP 3184806	B2	20010709		
	TW 464956	B	20011121	TW 1999-88100021	19990104
				US 1998-3106 A	19980106

AB Dual **work** function doping is provided by doping a selected no. of gate structures having self-aligned insulating layers on top of the structures through .gtoreq.1 side wall of the gate structures with a 1st cond. type to provide an array of gate structures, whereby some are doped with the 1st cond. type and others are doped with a 2nd cond. type. Also provided is an array of gate structures whereby the individual gate structures contain self-aligned insulating layers on their top portions and in which some of the gate structures are doped with a 1st cond. type and others are doped with a 2nd cond. type.
IT Electric insulators
(in dual **work** function doping of gate structures)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; dual **work** function doping of gate structures contg.)

L83 ANSWER 18 OF 63 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:651010 HCAPLUS
DN 132:8147
ED Entered STN: 13 Oct 1999
TI Process integration trends for **embedded DRAM**
AU Takato, H.; Koike, H.; Yoshida, T.; Ishiuchi, H.
CS Microelectronics Engineering Laboratory, Semiconductor Company, Toshiba Corporation, Yokohama, 235-0032, Japan
SO Proceedings - Electrochemical Society (1999), 99-18(ULSI Process Integration), 107-119
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
CC 76-14 (Electric Phenomena)
AB Issues and development trends respecting **embedded DRAM** (**eDRAM**) are reviewed by referring to real implementations for 0.5um, 0.35um and 0.25um generations. Chip performance has been progressively improved throughout the development of 0.5um, 0.35um and 0.25um **eDRAM**. However, the no. of process steps has increased compared to that for commodity DRAM. To avoid this problems and achieve the highest possible device performance, future directions of the **embedded DRAM** technologies, including MOSFET structure, memory cells, process cost and performance, are also discussed. For MOSFET structure, The logic-based MOSFET process offers more advantages than the DRAM-based one for future **eDRAM** generations. For memory cell structure, the trench cell is expected to be more useful for future **eDRAM** compared to the stacked cell. To combine the trench cell and logic-based MOSFET process, a new **embedded DRAM** technol. is proposed. This process technol. provides full process compatibility with high performance logic and min. no. of process steps, resulting in low process cost and short TAT(turn-around-time). DRAM array macro has been fabricated using this technol. with Co salicide, **dual work function** gate and aluminum bit-line processes, and excellent DRAM retention characteristics have been confirmed using neg. word-line bias scheme.

L91 ANSWER 19 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1998-332163 [29] WPIX
CR 1997-164527 [15]
DNN N1998-259268 DNC C1998-102859
TI Y-shaped storage capacitor for **DRAM** cell - is made with fewer photolithographic and etch steps increasing density and avoiding **stringer** problem.
IN LIANG, M; WANG, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
PI US 5759888 A 19980602 (199829)* 12p H01L021-8042
PRAI US 1996-590029 19960202; US 1996-734560 19961021

Manufacture of a Y-shaped storage capacitor on a substrate comprises forming an etch barrier (24) and an insulating layer (30) on the substrate (10), forming a contact hole and a trench around this hold and anisotropically etching the insulating layer through the trench. The contact hole and trench are covered with conductive polysilicon layer, a dielectric layer is formed to fill the trench and these layers are chemically mechanically polished to form a Y-shaped storage electrode (50). A capacitor dielectric (54) and a top electrode (56) are then formed to complete the capacitor.

Also claimed is a method of forming a DRAM cell having the Y- or T-shaped storage capacitor above.

USE - As capacitors of high capacitance in high density DRAM cells

ADVANTAGE - Fewer photo-lithographic and etch steps are needed, there is no problem with metal stringers and tighter ground rules are possible.

Dwg.4/9

FS CPI EPI
FA AB; GI

L83 ANSWER 58 OF 63 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1998-178492 [16] WPIX
DNN N1998-141275 DNC C1998-057257
TI Effective bit line to poly silicon gate **isolation** in **DRAM** - by **preventing** formation of poly silicon **stringers** along slope of bit line contact hole edge using pre-layer spacer to ease slope of contact edge.
IN HUANG, J; LIANG, M
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
PI US 5723374 A 19980303 (199816)* 8p H01L021-8242
PRAI US 1996-775049 19961227
AB US 5723374 A UPAB: 19980421

Forming a bit line contact in the fabrication of an integrated circuit device comprises: depositing a first polysilicon layer on the surface of a semiconductor substrate and patterning it to form a **gate electrode** wherein the bit line contact is to be formed adjacent to the **gate electrode**; forming a source/drain region associated with the **gate electrode** in the semiconductor substrate where the bit line contact is to be formed; forming first spacers on the sidewalls of the **gate electrode**; depositing a first insulating layer over the **gate electrode** and patterning it where the first insulating layer adjacent to the bit line contact has a first slope; depositing a second insulating layer over the first insulating layer; anisotropically etching the second insulating layer to leave second spacers on the sidewalls of the first insulating layer wherein the second spacers adjacent to the bit line contact have a second slope smaller than the first slope; depositing and patterning a second polysilicon layer overlying the **gate electrode**; depositing a first dielectric layer over the second polysilicon layer; depositing a third polysilicon layer overlying the first dielectric layer; etching away the third polysilicon layer and the first dielectric layer where the bitline contact is to be formed; depositing a second dielectric layer over the third polysilicon layer; etching a bit line contact opening through the second dielectric layer and the first insulating layer to the underlying semiconductor substrate where the bit line contact opening is separated from the third polysilicon by a thickness of the second dielectric layer; depositing a fourth polysilicon layer overlying the second dielectric layer and within the contact opening to form the bit line contact contacting the source/drain region.

USE - Fabrication of integrated circuit devices, a method of avoiding the formation of polysilicon stringers along the slope of a bit line contact opening.

ADVANTAGE - Avoids the formation of a polysilicon stringer along the slope of the bit line contact hole edge; maintains good isolation of the bit line to polysilicon gate in the fabrication of a **DRAM** integrated circuit device.

Dwg.10/10

FS CPI EPI

28/9/6

DIALOG(R)File 2:INSPEC

6142195 INSPEC Abstract Number: B1999-02-1265D-070, C1999-02-5320G-032

Title: Tutorial on DRAM fault modeling and test pattern design

Author(s): Cockburn, B.F.

Author Affiliation: Dept. of Electr. & Comput. Eng., Alberta Univ., Edmonton, Alta., Canada

Conference Title: Proceedings. International Workshop on Memory Technology, Design and Testing (Cat. No.98TB100236) p.66

Editor(s): Lepejian, D.; Lombardi, F.; Rajsuman, R.; Wik, T.

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Conference Title: Proceedings International Workshop on Memory Technology, Design and Testing

Conference Sponsor: IEEE Comput. Soc.; IEEE Comput. Soc. Tech. Committee on Test Technol.; IEEE Comput. Soc. Tech. Committee on VLSI; IEEE Solid-State Circuit Soc

Conference Date: 24-25 Aug. 1998 Conference Location: San Jose, CA,

Language: English Document Type: Conference Paper (PA)

Treatment: General, Review (G)

Abstract: Summary form only given, as follows. The problem of designing efficient and effective tests for semiconductor memories poses a daunting challenge to the test engineer. As commodity memory capacities approach the 1 Gb level by the end of this decade, testing cost becomes the largest component of the total cost of production. It is therefore essential to understand the precise nature of memory defects and failure mechanisms and to therefore be in the best position to design the most economic tests. A further complication in recent years has been the proliferation of specialized memory technologies, configurations and data access modes. This tutorial presentation focuses on reviewing the important fundamental concepts and techniques that are required to design high-quality tests for testing the cell **arrays** of **dynamic** random-access memories. Much of the memory testing literature has considered rather abstract functional fault models that appear to have little obvious justification in terms of observed faulty behaviors. In particular, much of the literature has dealt with fault models that would seem more appropriate for testing static rather than **dynamic** memory. The much larger production volume of **DRAMs** compared to that of SRAMs justifies specialized **DRAM** test methods. The topics covered in this presentation include the following: a brief review of **DRAM** architecture and operation; **DRAM**-specific defects and failure mechanisms; sources of soft failures and **array** noise; **DRAM**-specific fault models; the design of tests for the cell **array** ; tests for fault location and diagnosis; and recommended tests for **embedded DRAMs**. (2 Refs)

Subfile: B C

Descriptors: automatic test pattern generation; **DRAM** chips;

L83 ANSWER 19 OF 63 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:161045 HCAPLUS
DN 130:244800
ED Entered STN: 11 Mar 1999
TI Novel 0.44-.mu.m2 Ti salicide STI cell technology for high-density NOR flash memories and high performance **embedded** applications
AU Watanabe, H.; Yamada, S.; Tanimoto, M.; Matsui, M.; Kitamura, S.; Amemiya, K.; Tanzawa, T.; Sakagami, E.; Kurata, M.; Isobe, K.; Takebuchi, M.; Kanda, M.; Mori, S.; Watanabe, T.
CS Microelectronics Engineering Laboratory, Toshiba Corporation, Yokohama, 235, Japan
SO Technical Digest - International Electron Devices Meeting (1998) 975-978 CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-2 (Electric Phenomena)
AB This paper describes the key technol. to realize high-d. flash memory, which has quarter-micron shallow trench **isolation** (**STI**), Ti-silicided **polycryst. silicon** (**poly-Si**) gate and source/drain, and tungsten (W) **local interconnect** sourceline. An extremely small cell size of 0.44 .mu.m2 has been obtained with 0.25-.mu.m design rule. This cell size is about 30% redn. of conventional NOR flash cell. To minimize the cell size, the cell gate is patterned with a length of 0.25 .mu.m, which can be achieved by using channel erasing scheme. STI and 0.15-.mu.m floating gate sepn. can realize a 0.55-.mu.m bitline pitch. A W sourceline can reduce sourceline resistance and the no. of metal sourcelines in the array. In addn., **poly-Si** gate and active source/drain areas are Ti-silicided at both cells and peripheral transistors, which results in high-speed operation of memory array and peripheral circuits. This high-d. NOR cell technol. is essential in realizing a low-cost and high-performance flash **memory** and flash **embedded** logic devices.
IT **Memory devices**
(Ti salicide shallow trench isolation cell technol. for high-d. NOR flash memories and high-performance **embedded** applications)
IT Siliconizing
(salicide technol. = self-aligned siliconization; Ti salicide shallow trench isolation cell technol. for high-d. NOR flash memories and high performance **embedded** applications)

L86 ANSWER 5 OF 9 HCAPLUS

AN 1997:676580 HCAPLUS
DN 128:9268
ED Entered STN: 25 Oct 1997
TI Development of the 0.25-.mu.m W-polycide dual gate process using the stacked poly-Si structure
AU Tsukamoto, Masanori; Okamoto, Yutaka
CS MOS Process Dep., MOS LSI Div., Sony Semiconductor Co., Japan
SO Proceedings of the Sony Research Forum (1997), Volume Date 1996, 6th, 619-624
CODEN: PSRFFO; ISSN: 1340-3508
PB Soni K.K., Sogo Gijutsu Gurupu
DT Journal
LA English
CC 76-14 (Electric Phenomena)
AB W-polycide dual gate process with high-thermal-stability has been developed for quarter-micron device. In this work, gate lateral dopant diffusion between N+ and P+ gate electrodes was suppressed by using a stacked poly-Si structure. Furthermore, larger grains in the upper layer grew due to chem. oxide formation on the lower layer, and lateral dopant diffusion was suppressed. Boron penetration through gate oxide (Tox=5 nm) and gate poly-**Si** depletion were **prevented** with being annealed at 1000.degree.C for 10 s and then 850.degree.C for 30 min. The dual gate CMOS device has high performance at low-voltage operation and suitability for large scale **DRAM embedded** logic devices because of high thermal stability.

L98 ANSWER 3 OF 4 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1996-052149 [06] WPIX
DNN N1996-043721
TI **Polysilicon** field **ring** structure for power ICs - surrounds all diffusion wells that can contribute to field leakage by field rings biased to potential which blocks field induced leakage.
IN CHONGWOOK, C C; NIRAJ, R; CHOI, C C; RANJAN, N
PA (INRC) INT RECTIFIER CORP

PI	GB 2291257	A	19960117	(199606)*	16p	H01L029-06
	DE 19517975	A1	19960118	(199608)	7p	H01L027-105
	FR 2722611	A1	19960119	(199611)		H01L027-092
	JP 08046059	A	19960216	(199617)	6p	H01L021-8238
	SG 33410	A1	19961018	(199649)		H01L021-763
	US 5686754	A	19971111	(199751)	6p	H01L029-76
	IT 1275763	B	19971017	(199826)		H01L000-00
	GB 2291257	B	19990217	(199909)		H01L029-06

PRAI US 1994-274012 19940712; US 1996-660716 19960610
AB GB 2291257 A UPAB: 19960222
The structure has **polysilicon rings** (70,71) which shield the **silicon** surface beneath each **ring** from mobile ions in the IC plastic package (81) to prevent surface inversion. The rings completely surround each diffusion region to prevent field leakage in all directions. A **polysilicon ring** (71) is deposited to interrupt the field leakage path between diffusions (60,61). The ring receives an electrode (71a) tied to the lower potential in the high voltage region (40). The field leakage path between diffusions (62,63) is interrupted by a **polysilicon ring** (70) that receives an electrode (70a) tied to the highest potential in the region.

USE/ADVANTAGE - For MOSFETS, bipolar transistors, resistors, capacitors diodes. Prevents leakage from surface inversion induced by metal polysilicon signal lines and leakage caused by surface inversion induced by mobile ions in plastic package.
Dwg.2/3
ABEQ US 5686754 A UPAB: 19971222
A CMOS integrated circuit chip comprising a silicon substrate of one conductivity type and having at least one high voltage section aid at least one low voltage section; at least one **isolation** member for **isolating** said at least one high voltage section and said at least one low voltage section; a junction-receiving surface; a diffusion well of the other conductivity type in said junction-receiving surface; at least first and second spaced diffusions of said one conductivity type formed into said well and extending from said junction-receiving surface; at least third and fourth spaced diffusions of said other conductivity type formed in said junction-receiving surface; said first and second diffusions being included in first and second MOS transistors of said one conductivity type; said third and fourth diffusions being included in third and fourth MOS transistors of said other conductivity type; said first, second, third and fourth transistors being connected to define a CMOS circuit having a supply input terminal and a ground potential terminal; said junction-receiving surface of said substrate having an

insulation coating thereon; source, drain and gate signal lines **embedded** in said insulation coating; and a plastic chip housing having inherent contaminant ions therein in contact with said insulation coating; the improvement which comprises a plurality of **polysilicon rings embedded** in said insulation coating each of which at least partly surrounds at least one of said first, second, third and fourth diffusions; said rings being located beneath the source, drain and gate signal lines; said rings surrounding said first and second diffusions being connected to one of said supply terminal or said ground potential terminal, said one of said supply terminal or said ground potential terminal being said supply terminal when said one conductivity type is P-type and being said ground terminal when said one conductivity type is N-type so that the electrical potential of said rings surrounding said first and second diffusions shield said **silicon** surface beneath said **rings** from the electrical potential formed by contaminant ions in said plastic housing thereby preventing inversion of the **silicon** surface beneath said **rings**; said third and fourth diffusions being connected to the other of said supply terminal or said ground potential terminal so that the electrical potential of said rings surrounding said third and fourth diffusions shield said **silicon** surface beneath said **rings** from the electrical potential formed by contaminant ions in said plastic housing thereby preventing said inversion of the **silicon** surface beneath said **rings**.

Dwg.2/3

FS EPI

L83 ANSWER 22 OF 63 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:616984 HCAPLUS
DN 127:271320
ED Entered STN: 27 Sep 1997
TI Fabricating a dual-gate dielectric module for **memory devices** with **embedded** logic technology
IN Fang, Chung Hsin; Huang, Julie; Wang, Chen-jong; Liang, Mong-song
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5668035	A	19970916	US 1996-661259	19960610
				US 1996-661259	19960610

AB A method is described for forming a thin gate oxide for the peripheral circuits on a DRAM device, while providing a thicker oxide for the memory cells having a boosted word line architecture. The method avoids applying photoresist directly to the gate oxide, and thereby **prevents** contamination. A 1st gate oxide is formed on the device areas on the substrate. A 1st **polysilicon** layer is deposited and patterned, leaving portions over the memory cell areas. The 1st gate oxide is removed over the peripheral device areas, and is replaced by a thinner 2nd gate oxide. A 2nd **polysilicon** layer is deposited and patterned to remain over the peripheral device areas. The 1st and 2nd **polysilicon** layers, having essentially equal thicknesses, are coated with an insulating layer. The FET **gate electrodes** for both the peripheral and memory cell areas are simultaneously patterned from the 1st and 2nd **polysilicon** layers to complete the DRAM structure up to and including the **gate electrodes**.
IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**polycryst.**; fabricating a dual-gate dielec. module for memory devices contg.)

L91 ANSWER 20 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1998-086152 [08] WPIX
CR 1994-278947 [34]
DNN N1998-068467 DNC C1998-029094
TI Suppressing **stringer** formation in fabrication of **memory** array - by etching first and second poly silicon films in column to form cells by vertical plasma etching which also includes a horizontal component.
IN LUTTINGER, K A; PERRY, J R; SADJADI, S M R
PA (NASC) NAT SEMICONDUCTOR CORP
PI US 5705419 A 19980106 (199808)* 15p H01L021-265
PRAI US 1993-28026 19930308; US 1994-281525 19940727
AB US 5705419 A UPAB: 19980223

In the manufacture of a row and column array of memory cells on an oxide-coated top surface, including forming each cell with a first (14) and second (24) polySi layer, the formation of polySi stringers (42,44) between adjacent cells in a given column is avoided by forming the columns on the substrate before forming the second polySi layer (24); and selectively etching the columns and between the columns to form the rows using a plasma of HBr gas and Cl2 at a ratio greater than 1:1 so that the etching includes a vertical (anisotropic) component and a horizontal (isotropic) component. This ensures that polySi layers (14,24) between adjacent cells in the columns are removed, including stringers (42,44). Inert differential oxide (34) is left in place as a skeleton.

USE - Especially in manufacture of EPROMs (claimed) but also other memory cells such as EEPROMs, DRAMs and SRAMs.

ADVANTAGE - Formation of polySi stringers is prevented between adjacent cells with minimal undercutting of the sidewalls of the memory cells.

Dwg.5,7/14

FS CPI EPI

L91 ANSWER 8 OF 28 HCAPLUS
AN 1994:619529 HCAPLUS
DN 121:219529
ED Entered STN: 29 Oct 1994
TI Controllable isotropic plasma etching technique for the suppression of **stringers** in **memory** cells
IN Perry, Jeffrey R.; Sadjadi, S. M. Reza; Luttinger, Kristen A.
PA National Semiconductor Corp., USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5342801	A	19940830	US 1993-28026	19930308
	WO 9420981	A1	19940915	WO 1994-US2500	19940308
	US 5705419	A	19980106	US 1994-281525	19940727

AB In the manuf. of memory cells, esp. EPROMs, horizontal etching is controlled in a manner which prevents the formation of stringers between adjacent cells without undercutting the sidewalls of a memory cell.
IT Memory devices
(read-only, erasable programmable; controllable isotropic plasma etching technique for suppression of stringers in manuf. of)
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(polycryst.; isotropic plasma etching for suppression of stringers in manuf. of memory cells)

L110 ANSWER 10 OF 11 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1996-355875 [36] WPIX
DNN N1996-300171 DNC C1996-112097
TI Oxygen diffusion barrier in multilayer structures - comprises conductive refractory metal-silicon-nitrogen layer on top of conductive base, also preventing dopant out-diffusion.
IN AGNELLO, P D; CABRAL, C; GRILL, A; JAHNES, C V; LICATA, T J; ROY, R A
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

PI	EP 722190	A2	19960717	(199636)*	EN	10p	H01L029-49
	JP 08236479	A	19960913	(199647)		10p	H01L021-28
	US 5576579	A	19961119	(199701)		8p	H01L029-43
	US 5776823	A	19980707	(199834)			H01L021-28
	US 5796166	A	19980818	(199840)			H01L021-8238
	KR 204083	B1	19990615	(200063)			H01L021-322

PRAI US 1995-371627 19950112; US 1996-646583 19960508; US 1996-668241 19960621

A multilayered structure comprises a conducting base (20) with a refractory metal-Si-N diffusion barrier (12) on top, protecting the base from oxidn.. Also claimed is a method of preventing oxidn. of a silicon structure by depositing a refractory metal-Si-N diffusion barrier layer between the structure and an oxygen source. Further claimed is a method to prevent dopant diffusion in a gate stack having a doped Si layer and a refractory material silicide layer, with a layer of refractory metal-Si-N layer between.

USE - Used to protect a multilayer structure from oxidn., and to prevent out-diffusion of dopants from the base layer. The film can also be used as a base electrode for **DRAMS**, FERAMS and NVRAMS using high relative permittivity insulators.

ADVANTAGE - A low resistivity, thermally stable, oxidn. resistant dopant-diffusion barrier, allowing fabrication of **dual work** function polycide CMOS devices with a wide process window, is obtd..

Dwg.1/8

ABEQ US 5576579 A UPAB: 19970102

A multilayer structure comprising: a conducting base layer having a top surface, and a refractory metal-silicon-nitrogen layer adhered to the top surface of the conducting base layer, the refractory metal-silicon-nitrogen layer comprises alternating sub-layers of refractory metal-nitrogen and silicon-nitrogen each having a thickness of less than about 10 nm.

L91 ANSWER 22 OF 28 WPIX

AN 1994-303301 [37] WPIX

DNN N1994-238322

TI Conductive **stringer** suppression in **memory** cell mfr. - coating cells in nitride and replaces top nitride layer by poly II cap and row spaces are formed with nitride preventing **stringers**.

IN PERRY, J R; SADJADI, S M R; SADJADI, R S M

PA (NASC) NAT SEMICONDUCTOR CORP

PI	WO 9420989	A1	19940915	(199437)*	EN	18p	H01L027-115
	US 5427967	A	19950627	(199531)		8p	H01L021-70
	EP 689720	A1	19960103	(199606)	EN	1p	
	JP 08507657	W	19960813	(199702)		19p	H01L021-8247
	EP 689720	B1	20000726	(200036)	EN		H01L027-115
	DE 69425369	E	20000831	(200050)			H01L027-115
	KR 297018	B	20011024	(200236)			H01L027-115

PRAI US 1993-31373 19930311

AB WO 9420989 A UPAB: 19941109

The method of making memory cells to suppress electrically conductive stringers includes forming a nitride layer. The memory cell (42) is one of many in a row and column arrangement. Each cell is formed on a silicon substrate (12) with an oxide layer (14). Further layers of poly I (16), ONO (18, 20, 22) are added.

During the formation of the cell, a horizontal and vertical (50) layer of nitride is formed. The top layer of the nitride is removed and replaced by a layer of poly II (20). A differential oxide layer (34) is formed within the column spaces. Row spaces are then formed.

USE - E.g. in EPROM.

Dwg.7/9

ABEQ US 5427967 A UPAB: 19950810

Each of the cells includes an array of different layers on the oxide coated top surface of the substrate including, in particular, the polysilicon layer. The method prevents formation of polysilicon stringers between individual cells during their manufacture.

This method is carried out by first forming the columns before the rows are formed such that continuous sidewalls of the columns are exposed to the ambient surroundings. Thereafter, these sidewalls are coated with protective layers, specifically layers of nitride.

USE/ADVANTAGE - For manufacturing a group of memory cells or devices on a common oxide coated silicon substrate such that the cells are arranged in rows and columns with row and column spaces separating the individual cells from one another.

Dwg.7/9

L91 ANSWER 23 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1994-095891 [12] WPIX
DNN N1994-075209
TI Semiconductor device, e.g. 64 megabit **DRAM** or SRAM - has multilayered contact structure including BPSG planarising layer and is self aligned and free of residual **stringers**.
IN CHANG, S; SHIN, Y
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
PI JP 06045329 A 19940218 (199412)* 6p H01L021-3205
US 5414302 A 19950509 (199524)B 7p H01L023-48
PRAI KR 1992-3559 19920304
AB US 5414302 A UPAB: 19950626 ABEQ treated as Basic
In a semiconductor device having a contact pad structure in a via of an inter-insulating layer, the contact pad comprises a conductive layer (17') in the via, an insulating planarising layer (23) filling the via, and a second conductive layer (28') on the planarising layer, connected to the first conductive layer through the latter's upper end portion.
USE - For contacts in high density semiconductor devices such as 64 Mbit DRAMs and SRAMs.
ADVANTAGE - Electrical connection to the upper pad is easy, no stringers are left, and reliability is increased.
Dwg.3F/3
AB JP 06045329 A UPAB: 19940510
Dwg.3/5

L15 ANSWER 25 OF 26 WPIX
AN 1991-312018 [43] WPIX
DNN N1991-239147 DNC C1991-135095
TI Gate insulation region formation for field effect gate device - comprises forming on substrate, insulator region, partially masked **poly-silicon** layer and etched conductive region.
IN BISWAL, M; BLAIR, C S; ILDEREM, V; IRANMANESH, A A; JEROME, R C; RAJEEVA, L; SOLHEIM, A G
PA (NASC) NAT SEMICONDUCTOR CORP
PI

EP 452720	A	19911023	(199143)*			
JP 04226066	A	19920814	(199239)	17p	H01L027-092	<--
US 5338694	A	19940816	(199432)	15p	H01L021-265	<--
US 5338696	A	19940816	(199432)	17p	H01L021-265	<--
EP 452720	A3	19941026	(199534)			
US 5661046	A	19970826	(199740)		H01L021-265	<--
KR 223098	B1	19991015	(200108)		H01L027-10	<--

PRAI US 1990-502943 19900402; US 1992-847876 19920309; US 1993-22708 19930301; US 1994-285839 19940804
AB EP 452720 A UPAB: 19930928
A method of forming a gate insulating region for a field effect gate comprise forming: a) insulator region on semiconductor substate surface; b) first **polysilicon** layer on insulator; c) mask on portions of **polysilicon** layer, which define gate regions; d) **polysilicon** and insulator from unprotected regions of mask; e) conductive region along surface; and f) etching conductive region to form gate.

Method for fabricating field effect device of selected threshold voltage, contg. channel regions of first and second conductivity type, comprising: a) in substrate contg. surface of first and second regions, implant using first dopant in first region and second dopant into both regions; b) forming gate oxide regions on both regions and c) forming conductive gates on gate oxide regions.

USE/ADVANTAGE - Semiconductor devices can be made with improved performance, reduced size, and of simpler fabrication. Devices can be used with high performance Emitter Coupled Logic (ECL) standard cell designs, multiport 6 transistor memory cell, gate array designs with **embedded memory** etc. It has improved gate oxide formation and adjusting of the threshold voltage whilst also providing method of forming a base region in bipolar devices as a channel region in field effect devices in a BiCMO5 process.
1/27
ABEQ US 5338694 A UPAB: 19940928
Semiconductor devices are mfd. by (a) implanting n-type deposits to form an n-type buried layer in a p-type substrate, for PMOS and bipolar transistors, (b) forming a p-type buried layer for an NMOS-transistor and p-type channel stops adjacent a 1st region, (c) forming an n-type epitaxial Si layer, (d) forming field oxide regions adjacent the 1st, 2nd and 3rd regions, as well as between a sink and a base region of the 1st region, (e) implanting n-type dopants into the sink region to a 1st concn., (f) implanting p-type dopants into the 3rd region to a 2nd concn.,

(g) implanting p-type dopants into the 2nd and 3rd regions to adjust the threshold voltages of the NMOS and PMOS transistors, (h) forming an insulator region comprising a gate oxide layer, (i) forming a 1st **poly-Si** layer, (j) forming a mask to define gate regions of FETs, (k) **removing** the **poly-Si** and insulator from unprotected regions, (l) forming a conductive region above the insulator comprising a 2nd **poly-Si** layer; (m) etching the conductive region to form the gates above the insulator regions, by masking and implanting n-type and p-type dopants into the 2nd **poly-Si** layer, and forming emitter, base and collector contacts for the bipolar transistors, and source and drain contacts for the NMOS and PMOS transistors, then (n) implanting n-type dopant into the NMOS to form a lightly doped diffusion, (o) implanting B in the PMOS, (p) forming sidewall oxide on all the transistor contacts, (q) removing sidewall oxide from exposed regions, (r) p-type doping of 1st and 3rd regions, (s) n-type doping of 2nd regions, (t) forming a refractory metal layer across the 1st, 2nd and 3rd regions and heating to form metal silicide where it meets **Si**, (u) **removing** unreacted metal, and (v) forming an interconnect system between the transistors.

ADVANTAGE - Improved performance, reduced size and more simple fabrication.

Dwg.2v/4

ABEQ US 5338696 A UPAB: 19940928

The semiconductor structure is formed by (a) masking regions including at least base regions of bipolar transistors, (b) implanting with a 1st type dopant to provide channel regions with 1st characteristics, (c) forming a **poly-Si** layer over at least the base regions, (d) masking regions including at least the channel regions of FETs, (e) implanting the **poly-Si** layer with a 1st-type dopant, and (f) diffusing dopants from the **poly-Si** layer into underlying Si to provide at least a portion of the base regions of the bipolar transistors with 2nd characteristics. The 1st and 2nd characteristics are dopant concns. or implant depths. The 1st dopant is implanted at 30-100 KeV and the 2nd dopant at 30-50 KeV.

USE/ADVANTAGE - Used to form BiCMOS devices. The devices have improved performance, reduced size and can be fabricated more simply and economically.

Dwg.1/5

ABEQ US 5661046 A UPAB: 19971006

A method of fabricating BiCMOS devices on a substrate with a selected threshold voltage for field effect devices, a first portion of said BiCMOS devices including said field effect devices having a channel region of a first conductivity type, a second portion of said BiCMOS devices including said field effect devices having a channel region of a second conductivity type, a third portion of said BiCMOS devices including a bipolar region, the method comprising the steps of:

a) in the substrate having a surface with first and second regions being adjacent to said bipolar region, implanting a first dopant in said first region, said first dopant of said first conductivity type;

b) implanting said first and said second regions with a second dopant, said second dopant of said second conductivity type, said first

region having a net dopant concentration of said first conductivity type;

c) forming gate oxide regions on said first and said second regions; and

d) forming conductive gates on said gate oxide regions, said first region comprising said channel region of said first conductivity type, said second regions comprising said channel regions of said second conductivity type;

and wherein the step of implanting said first dopant in said first region is preceded by the step of providing a well region having the second conductivity dopant below said second regions, the threshold voltage of said field effect devices formed in said second regions is set by up-diffusing dopant from said well region in combination with said implant of said second dopant.

L91 ANSWER 24 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1993-017576 [02] WPIX
DNN N1993-013438 DNC C1993-008034
TI Integrated circuit with double poly silicon capacitors and **MOSFET** devices - produced without **stringers** by simultaneous formation of the gate electrode and bottom capacitor plate which allows precise dimensional control.
IN CHI, K C
PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG PTE LTD
PI US 5173437 A 19921222 (199302)* 7p H01L021-70
PRAI US 1991-739222 19910801
AB US 5173437 A UPAB: 19930924
Fabricating an IC having double polycrystalline Si capacitors and MOSFET devices which are compatible to 1 micron or less processing comprises : forming a pattern of recessed oxide isolation on the surface of a monocrystalline Si substrate which separates surface regions of Si from other regions; forming a gate dielectric layer on the surface of the surface regions of the Si; forming a 1st. polycrystalline Si layer (I), over the gate dielectric layer and the isolation pattern, which has a doping concn. for imparting high conductivity; forming an undoped interpoly dielectric layer of the surface of layer (I); forming a 2nd. polycrystalline layer (II), over the interpoly dielectric layer which has a doping concn. for high conductivity; patterning layer (II) using a 1st. resist mask and etch to leave only the top plate of the capacitor in layer (II); removing the interpoly dielectric layer except where it is located beneath the top plate by using the top plate as the etching mask; pattterning layer (I) using a 2nd. resist mask and etch to leave only a bottom plate of the capacitor and the gate electrode of the transistor in layer (I); and removing 2nd. resist masking layers.
USE/ADVANTAGE - Method for making a double polycrystalline Si capacitor and FET IC, which will not produce ''stringers''.
7/8
FS CPI EPI
FA AB; GI

L98 ANSWER 4 OF 4 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1983-790042 [42] WPIX
DNN N1983-183714 DNC C1983-100011
TI Complementary MOS transistors prodn. on **silicon** monocrystal - sepd. by protective **ring** by masking, doping and diffusion, useful at high voltage.
IN CEROFOLINI, G
PA (SGSA) SGS ATES COMPONENTI ELTRN SPA; (SGSA) SGS ATES COMPONENTIELTRN SPA;
PI

DE 3312720	A	19831013	(198342)*	18p	
FR 2525030	A	19831014	(198346)		
GB 2120844	A	19831207	(198349)		
NL 8301229	A	19831101	(198349)		
JP 58202562	A	19831125	(198402)		
US 4468852	A	19840904	(198438)		
GB 2120844	B	19850925	(198539)		
IT 1210872	B	19890929	(199144)		
NL 188607	B	19920302	(199212)	8p	
DE 3312720	C	19920917	(199238)	8p	H01L027-092
JP 04079142	B	19921215	(199302)	18p	H01L027-092

AB DE 3312720 A UPAB: 19930925
In the prodn. of a pair of complementary MOS (CMOS) transistors on a monocrystalline Si substrate, from which each transistor is sepd. by a protective ring, the 2 zones are defined on the substrate, sepd. by an intermediate zone, and the intermediate zone is n-doped to form a first protective **ring**. A **polycrystalline Si** mask
is formed on the substrate, covering pt. of the intermediate zone and a first pt. of both zones. The second zone is p-doped, then the array is heated in a non-oxidising atmos. to a first temp. of a first time to effect diffusion of the n- and p-dopants into the substrate. The unmasked pt. of the intermediate zone is strongly p-doped, then the mask is removed.

The array is then heated to a second, lower temp. for a certain time to effect diffusion of the p-dopant only to a certain depth. A protective film of SiO2 is formed on the whole of the intermediate zone and the 2 CMOS devices are formed in both zones on the substrate.

These CMOS transistors are suitable for operation at relatively high voltage. They have a constant threshold voltage, i.e. not dependent on the channel width, and at least as high integration density as usual.
0/10

ABEQ DE 3312720 C UPAB: 19930925
In the process, two regions (4, 6) are marked off on the substrate for the two transistors, separated by an intermediate zone (7) which is doped with material leading to the conductivity of the first type (n), provided the first part of the protecting ring, a mask (15) is formed on the substrate. The mask covers the region (6) and a part of the intermediate zone. (p) the region not covered by the mask is doped with material leading to conductivity of the second type (e) and a recess is formed for on the transistors. The uncovered part of the intermediate zone is doped, forming a second part of the protecting ring. The mask is then removed, and the doping material is diffused by heat into the substrate. A protecting layer

of silicon dioxide is deposited on the intermediate zone.
USE/ADVANTAGE - Forming for a pair of MOS transistors (4, 6) on a monocrystalline silicon substrate (2), each transistor being **isolated** by a protecting ring. There is a constant threshold voltage, independent of the channel width, and a density of integration at least as good as that produced by known methods.
6/10

ABEQ GB 2120844 B UPAB: 19930925
A method of forming on a substrate of monocrystalline silicon a pair of complementary MOS transistors each insulated by a respective guard ring, comprising the steps of: defining first and second areas of the substrate separated from one another by an intermediate zone; doping the intermediate zone with impurities of a first type of conductivity for the formation of a first guard ring; forming on the substrate a mask of polycrystalline silicon which covers part of the intermediate zone and the first area; doping the second area with impurities of a second type of conductivity; heating in a non-oxidising atmosphere at a first predetermined temperature for a period sufficient to cause the diffusion in the substrate of the impurities of the first and second types of conductivity **embedded** in the substrate in the previous steps; doping part of the intermediate zone which is not protected by the polycrystalline silicon mask with impurities of the second type of conductivity at a concentration such as to obtain, at the end of the process, a second guard ring highly doped with impurities of the second type; removing the mask; heating to a second predetermined temperature which is lower than the first for a period sufficient to cause the diffusion of the impurities of the second type of conductivity alone up to a predetermined depth, these being **embedded** in the substrate in the previous doping step: formating a protective layer of silicon dioxide over the entire intermediate zone; and formating two complementary MOS devices in the substrate in the two areas.

ABEQ US 4468852 A UPAB: 19930925
CMOS FET with self-aligned guard rings is made by forming two regions of Si nitride above spaced regions of an n-type substrate overlying a thin oxide layer. As ions are implanted through the oxide in areas not covered by the patches and one patch and adjoining oxide are marked by Si. B ions are introduced initially at a low concn. and high energy level to penetrate the oxide layer and the second nitride region and then at a high concn. and low energy level after heat treatment in a non-oxidising atmos.
A p well is formed bounded by an n+ guard zone which is partly under-reached. The exposed area of the guard zone is converted to p+ conductivity by the second stage bombardment. Further heat treatment at a lower temp. expands the p+ area into a channel stop which bounds the p-well. The polycrystalline layer is removed and the oxide layer grown and partially removed by deposition of polycrystalline Si on residues of the layer to form insulated gates source and drain areas are formed on the p-well and n-type pedestal bounded by an n+ channel stop.
ADVANTAGE - Large ratio of channel width to overall width.

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